Engineering
Circuit Analysis

Fourth Edition

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We shall not attempt the solution of these equations at this time. It is worthwhile pointing out, however, that when the two voltage forcing functions are sinusoidal functions of time it will be possible to define a voltage-current ratio (called impedance) or a current-voltage ratio (called admittance) for each of the three passive elements. The factors operating on the two node voltages in the equations above will then become simple multiplying factors, and the equations will be linear *algebraic* equations once again. These we may solve by determinants or a simple elimination of variables as before.

Drill Problem	**4-6.** (*a*) Find L_{eq} in Fig. 4-19*a*. (*b*) Find C_{eq} in Fig. 4-19*b*. (*c*) Find i_s in Fig. 4-19*c* if $i_L = 0.03 \sin 5000t$ A. *Ans:* 2.62 H; 6.91 μF; 0.015 $\sin 5000t$ A
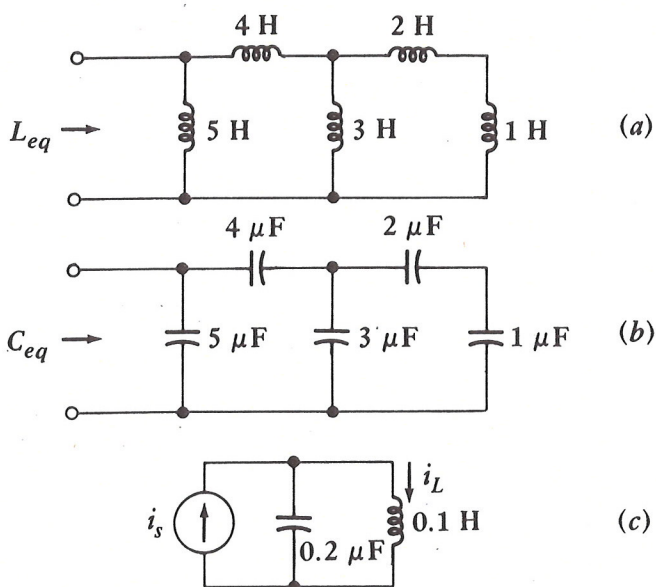
**Fig. 4-19:** See Drill Prob. 4-6.

4-6
Duality

Duality has been mentioned earlier in connection with resistive circuits and more recently in the discussion of inductance and capacitance; the comments made were introductory and, like the man who tried to pet the alligator, a little offhand. Now we may make an exact definition and then use the definition to recognize or construct dual circuits and thus avoid the labor of analyzing both a circuit and its dual.

We shall define duality in terms of the circuit equations. Two circuits are *duals* if the mesh equations that characterize one of them have the same mathematical form as the nodal equations that characterize the other. They are said to be *exact duals* if each mesh equation of the one circuit is numerically identical with the corresponding nodal equation of the other; the current and voltage variables themselves cannot be identical, of course. *Duality* itself merely refers to any of the properties exhibited by dual circuits.

Let us interpret the definition and use it to construct an exact dual circuit
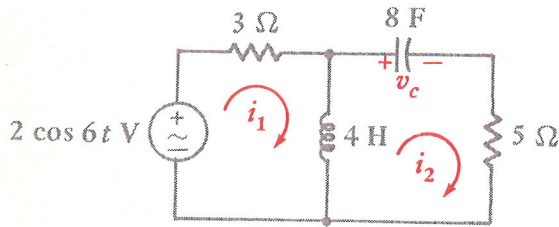
Fig. 4-20: A given circuit to which the definition of duality may be applied to determine the dual circuit.
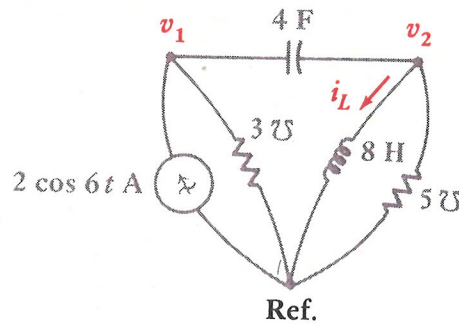
Fig. 4-21: The exact dual of the circuit of Fig. 4-20.

by writing the two mesh equations for the circuit shown in Fig. 4-20. Two mesh currents i_1 and i_2 are assigned, and the mesh equations are

$$3i_1 + 4\frac{di_1}{dt} - 4\frac{di_2}{dt} = 2 \cos 6t \tag{17}$$

$$-4\frac{di_1}{dt} + 4\frac{di_2}{dt} + \frac{1}{8}\int_0^t i_2 \, dt + 5i_2 = -10 \tag{18}$$

It should be noted that the capacitor voltage v_C is assumed to be 10 V at $t = 0$.

We may now construct the two equations which describe the exact dual of the given circuit. We wish these to be nodal equations, and we thus begin by replacing the mesh currents i_1 and i_2 in Eqs. (17) and (18) by two node-to-reference voltages v_1 and v_2. We obtain

$$3v_1 + 4\frac{dv_1}{dt} - 4\frac{dv_2}{dt} = 2 \cos 6t \tag{19}$$

$$-4\frac{dv_1}{dt} + 4\frac{dv_2}{dt} + \frac{1}{8}\int_0^t v_2 \, dt + 5v_2 = -10 \tag{20}$$

and we now seek the circuit represented by these two nodal equations.

Let us first draw a line to represent the reference node, and then we may establish two nodes at which the positive references for v_1 and v_2 are located. Equation (19) indicates that a current source 2 cos 6t is connected between node 1 and the reference node, oriented to provide a current entering node 1. This equation also shows that a 3-℧ conductance appears between node 1 and the reference node. Turning to (20), we first consider the nonmutual terms, or those terms which do not appear in (19), and they instruct us to connect an 8-H inductor and a 5-℧ conductance (in parallel) between node 2 and the reference. The two similar terms in (19) and (20) represent a 4-F capacitor present mutually at nodes 1 and 2; the circuit is completed by connecting this capacitor between the two nodes. The constant term on the right side of (20) is the value of the inductor current at $t = 0$; thus, $i_L(0) = 10$ A. The dual circuit is shown in Fig. 4-21; since the two sets of equations are numerically identical, the circuits are exact duals.

Dual circuits may be obtained more readily than by the above method, for the equations need not be written. In order to construct the dual of a given circuit, we think of the circuit in terms of its mesh equations. With each mesh we must associate a nonreference node, and, in addition, we must supply the reference node. On a diagram of the given circuit we therefore place a node in the center of each mesh and supply the reference node as a line near the diagram or a loop enclosing the diagram. Each element which appears jointly in two meshes is a *mutual* element and gives rise to identical terms, except for sign, in the two corresponding mesh equations. It must be replaced by an element which supplies the dual term in the two corresponding nodal equations. This dual element must therefore be connected directly between the two nonreference nodes which are within the meshes in which the given mutual element appears. The nature of the dual element itself is easily determined; the mathematical form of the equations will be the same only if inductance is replaced by capacitance, capacitance by inductance, conductance by resistance, and resistance by conductance. Thus, the 4-H inductor which is common to meshes 1 and 2 in the circuit of Fig. 4-20 appears as a 4-F capacitor connected directly between nodes 1 and 2 in the dual circuit.

Elements which appear only in one mesh must have duals which appear between the corresponding node and the reference node. Referring again to Fig. 4-20, the voltage source $2 \cos 6t$ V appears only in mesh 1; its dual is a current source $2 \cos 6t$ A which is connected only to node 1 and the reference node. Since the voltage source is clockwise-sensed, the current source must be into-the-nonreference-node-sensed. Finally, provision must be made for the dual of the initial voltage present across the 8-F capacitor in the given circuit. The equations have shown us that the dual of this initial voltage across the capacitor is an initial current through the inductor in the dual circuit; the numerical values are the same, and the correct sign of the initial current may be determined most readily by considering both the initial voltage in the given circuit and the initial current in the dual circuit as sources. Thus, if v_C in the given circuit is treated as a source, it would appear as $-v_C$ on the right side of the mesh equation; in the dual circuit, treating the current i_L as a source would yield a term $-i_L$ on the right side of the nodal equation. Since each has the same sign when treated as a source, then, if $v_C(0) = 10$ V, $i_L(0)$ must be 10 A.

The circuit of Fig. 4-20 is repeated in Fig. 4-22, and its exact dual is constructed on the circuit diagram itself by merely drawing the dual of each
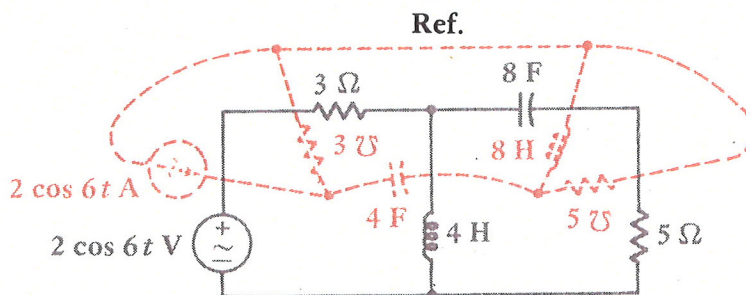
Fig. 4-22: The dual of the circuit of Fig. 4-20 is constructed directly from the circuit diagram.

Fig. 4-23: (a) The dual (in color) of a given circuit (in black) is constructed on the given circuit. (b) The dual circuit is drawn in more conventional form.

(a)   (b)
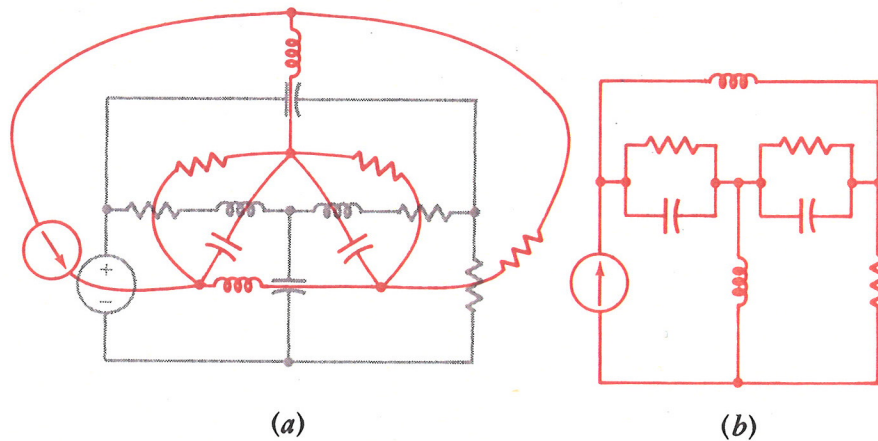
given element between the two nodes which are centered in the two meshes which are common to the given element. A reference node which surrounds the given circuit may be helpful. After the dual circuit is redrawn in more standard form, it appears as shown in Fig. 4-21.

An additional example of the construction of a dual circuit is shown in Figs. 4-23a and b. Since no particular element values are specified, these two circuits are duals, but not necessarily exact duals. The original circuit may be recovered from the dual by placing a node in the center of each of the five meshes of Fig. 4-23b and proceeding as before.

The concept of duality may also be carried over into the language by which we describe circuit analysis or operation. One example of this was discussed previously in Sec. 4-4, and the duals of several words appeared there. Most of these pairs are obvious; whenever there is any question as to the dual of a word or phrase, the dual circuit may always be drawn or visualized and then described in similar language. For example, if we are given a voltage source in series with a capacitor, we might wish to make the important statement, "the voltage source causes a current to flow through the capacitor"; the dual statement is, "the current source causes a voltage to exist across the inductor." The dual of a less carefully worded statement, such as, "the current goes round and round the series circuit," often requires a little inventiveness.[3]

Practice in using dual language can be obtained by reading Thévenin's theorem in this sense; Norton's theorem should result.

We have spoken of dual elements, dual language, and dual circuits. What about a dual *network*? Consider a resistor R and an inductor L in series. The dual of this two-terminal network exists and is most readily obtained by connecting some ideal source to the given network. The dual circuit is then obtained as the dual source in parallel with a conductance G, $G = R$, and a capacitance C, $C = L$. We consider the dual network as the two-terminal network that is connected to the dual source; it is thus a pair of terminals between which G and C are connected in parallel.

Before leaving the definition of duality, it should be pointed out that dual-

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[3] Someone has suggested, "the voltage is across all over the parallel circuit."

ity is defined on the basis of mesh and nodal equations. Since nonplanar circuits cannot be described by a system of mesh equations, a circuit which cannot be drawn in planar form does not possess a dual.

We shall use duality principally to reduce the work which we must do to analyze the simple standard circuits. After we have analyzed the series RL circuit, then the parallel RC circuit requires less attention, not because it is less important, but because the analysis of the dual network is already known. Since the analysis of some complicated circuit is not apt to be well known, duality will usually not provide us with any quick solution.

Drill Problem	**4-7.** Write the single mesh equation for the circuit of Fig. 4-24a and show, by direct substitution, that $i = 4e^{-2000t}$ A is a solution. Knowing this, refer to Fig. 4-24b and find: (a) i_1; (b) i_2. *Ans:* $80e^{-2000t}$; $-48e^{-2000t}$ A
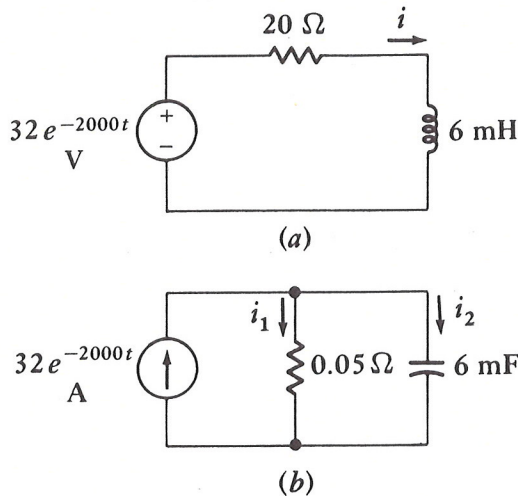
Fig. 4-24: See Drill Prob. 4-7.

4-7
Linearity and its consequences again

In the previous chapter we learned that the principle of superposition is a necessary consequence of the linear nature of the resistive circuits which we were analyzing. The resistive circuits are linear because the voltage-current relationship for the resistor is linear and Kirchhoff's laws are linear.

We now wish to show that the benefits of linearity apply to RLC circuits as well. In accordance with our previous definition of a linear circuit, these circuits are also linear because the voltage-current relationships for the inductor and capacitor are linear relationships. For the inductor, we have

$$v = L\frac{di}{dt}$$

and multiplication of the current by some constant K leads to a voltage which is also greater by a factor K. In the integral formulation,

$$i = \frac{1}{L}\int_{t_0}^{t} v\, dt + i_L(t_0)$$

it can be seen that, if each term is to increase by a factor of K, then the initial

value of the current must also increase by this same factor. That is, the factor K applies not only to the current and voltage at time t but also to their past values.

A corresponding investigation of the capacitor shows that it too is linear. Thus, a circuit composed of independent sources, linear dependent sources, and linear resistors, inductors, and capacitors is a linear circuit.

In this linear circuit the response is again proportional to the forcing function. The proof of this statement is accomplished by first writing a general system of integrodifferential equations, say, in terms of loop currents. Let us place all the terms having the form of Ri, $L \, di/dt$, and $(1/C) \int i \, dt$ on the left side of each equation and keep the independent source voltages on the right side. As a simple example, one of the equations might have the form

$$Ri + L \frac{di}{dt} + \frac{1}{C} \int_{t_0}^{t} i \, dt + v_C(t_0) = v_s$$

If every independent source is now increased by a factor K, then the right side of each equation is greater by the factor K. Now each term on the left side is either a linear term involving some loop current or an initial capacitor voltage. In order to cause all the responses (loop currents) to increase by a factor K, it is apparent that we must also increase the initial capacitor voltages by a factor K. That is, we must treat the *initial capacitor voltage as an independent source voltage* and increase it also by a factor K. In a similar manner, initial inductor currents must be treated as independent source currents in nodal analysis.

The principle of proportionality between source and response is thus extensible to the general RLC circuit, and it follows that the principle of superposition is also applicable. It should be emphasized that initial inductor currents and capacitor voltages must be treated as independent sources in applying the superposition principle; each initial value must take its turn in being rendered inactive.

Before we can apply the superposition principle to RLC circuits, however, it is first necessary to develop methods of solving the equations describing these circuits when only one independent source is present. At this time we should feel convinced that a linear circuit will possess a response whose amplitude is proportional to the amplitude of the source. We should be prepared to apply superposition later, considering an inductor current or capacitor voltage specified at $t = t_0$ as a source which must be killed when its turn comes.

Thévenin's and Norton's theorems are based on the linearity of the initial circuit, the applicability of Kirchhoff's laws, and the superposition principle. The general RLC circuit conforms perfectly to these requirements, and it follows, therefore, that all linear circuits which contain any combinations of independent voltage and current sources, linear dependent voltage and current sources, and linear resistors, inductors, and capacitors may be analyzed with the use of these two theorems, if we wish. It is not necessary to

repeat the theorems here, for they were previously stated in a manner that is equally applicable to the general *RLC* circuit.
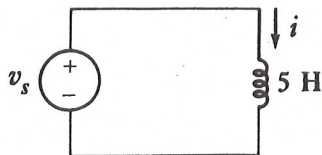
Problems

1 Let v_L and i_L be assigned to a 20-mH inductor so as to satisfy the passive sign convention. (*a*) If $i_L = 12e^{-5t} \cos 10t$ A, find v_L at $t = 0.1$ s. (*b*) If $i_L = 8(e^{-6t} - e^{-2t})$ A, find $v_{L,max}$ and the value of time at which it occurs.

2 The current through a 2-mH inductor is $i_L = 0$ for $t < 0$, $500t$ A for $0 < t < 10$ ms, $10 - 500t$ A for $10 < t < 30$ ms, -5 A for $30 < t < 40$ ms, and $-5 \cos^2 [50\pi(t - 0.04)]$ A for $40 < t < 50$ ms. For the interval, $0 < t < 50$ ms: (*a*) sketch i_L vs. t; (*b*) sketch v_L vs. t, assuming the passive sign convention.

3 In Fig. 4-25, let $v_s(t) = 20\,t$ V for $0 < t < 3$ s, and $v_s = 0$ for $t < 0$ and $t > 3$. Find: (*a*) the value of i at $t = 4$ s; (*b*) the energy stored in the inductor at $t = 2$ s; (*c*) the power entering the inductor at $t = 2$ s.

4 The current in a 0.4-H inductor is zero for $t < 0$ and $3te^{-0.1t}$ A for $t > 0$. (*a*) At what instant is maximum power being delivered to the inductor? (*b*) At what instant is the energy stored in the inductor a maximum?

5 In the circuit of Fig. 4-26, let $v_s = 100 \cos 500t$ V for $t > -0.5$ s, and let $i_L(0) = -1$ A. (*a*) Find $i_s(t)$. (*b*) Find $w_L(t)$ at $t = 1$ ms.
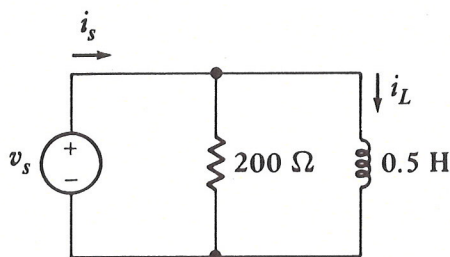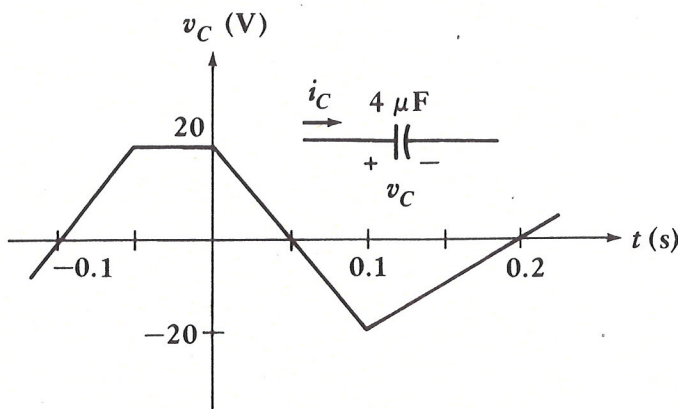
Fig. 4-25: See Prob. 3.

Fig. 4-26: See Prob. 5.

6 (*a*) If $v_C(t)$ is given by the waveform shown in Fig. 4-27, sketch $i_C(t)$ for $-0.1 < t < 0.2$ s. (*b*) Sketch the power entering the capacitor over the same time interval.

Fig. 4-27: See Prob. 6.

7 The current through a 0.2-μF capacitor is $60 \cos (10^4 t + 36°)$ mA for all time. The average voltage across the capacitor is zero. (*a*) What is the maximum value of energy stored in the capacitor? (*b*) What is the first nonnegative value of t at which maximum energy is stored?

8 The energy stored in a 50-μF capacitor is given as $w_C(t) = 2e^{-50t}$ J for $t \geq 0$. Find the capacitor voltage, current, and absorbed power at $t = 30$ ms.

9 In the circuit of Fig. 4-10a, let $R = 1$ MΩ, $C = 1$ μF, $R_i = \infty$, and $R_o = 0$. Suppose that we wish the output to be $v_o(t) = e^{-10t} - 1$ V. Differentiate Eq. (16) to obtain the necessary $v_s(t)$ if: (a) $A = 1000$; (b) A is infinite.

10 Interchange the location of R and C in the circuit of Fig. 4-10a and assume that $R_i = \infty$, $R_o = 0$, and $A = \infty$ for the op-amp. (a) Find $v_o(t)$ as a function of $v_s(t)$. (b) Obtain an equation relating $v_o(t)$ and $v_s(t)$ if A is not assumed to be infinite.

11 In the circuit shown in Fig. 4-28, $v_C(t) = 4te^{-2t}$ V. At $t = 0.5$ s, find the value of: (a) the energy stored in the capacitor; (b) the energy stored in the inductor; (c) v_s.

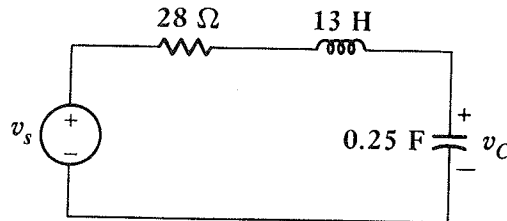**Fig. 4-28:** See Prob. 11.

12 (a) If each inductance in the network of Fig. 4-29 is 1 H, find the equivalent inductance at a-b. (b) Replace each inductor by a 1-F capacitor and find C_{eq}.
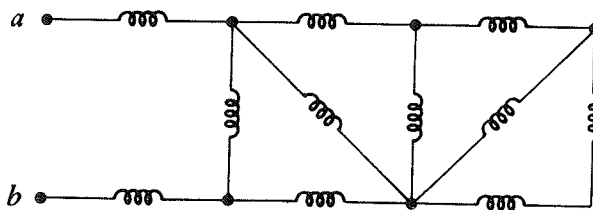

Fig. 4-29: See Prob. 12.

13 Find the equivalent inductance offered at terminals a-b in Fig. 4-30 if terminals x-x' are: (a) open-circuited; (b) short-circuited.
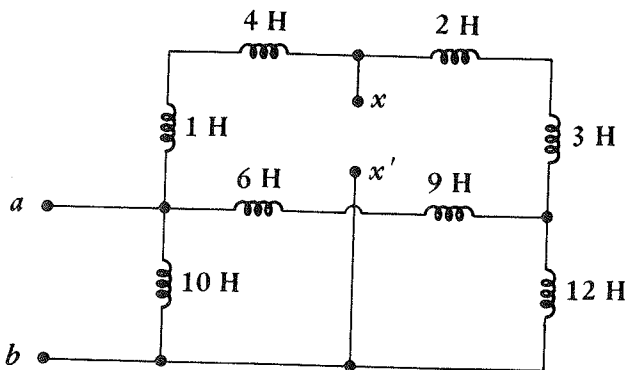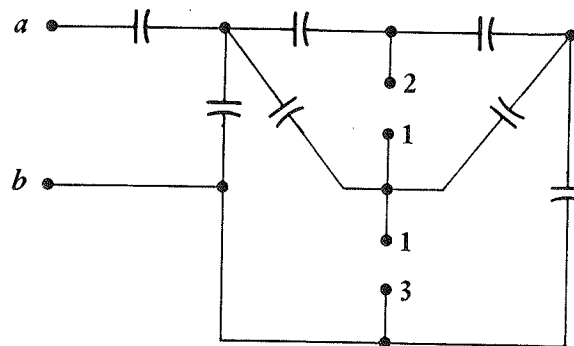

Fig. 4-30: See Prob. 13.

Fig. 4-31: See Prob. 14.

14 Each capacitor in Fig. 4-31 is 1 μF. Find C_{eq} at a-b if: (a) 1-2 and 1-3 are both open-circuited; (b) 1-2 and 1-3 are both short-circuited; (c) 1-2 is open-circuited and 1-3 is short-circuited; (d) 1-2 is short-circuited and 1-3 is open-circuited.

15 Given a bucketful of 1-nF capacitors, show how an equivalent capacitance of 0.7 nF might be obtained. Use as few capacitors as possible.

16 For the circuit of Fig. 4-32, find: (a) w_C; (b) w_L; (c) the current in each circuit element; (d) the voltage across each circuit element.