Engineering Circuit Analysis

Fourth Edition

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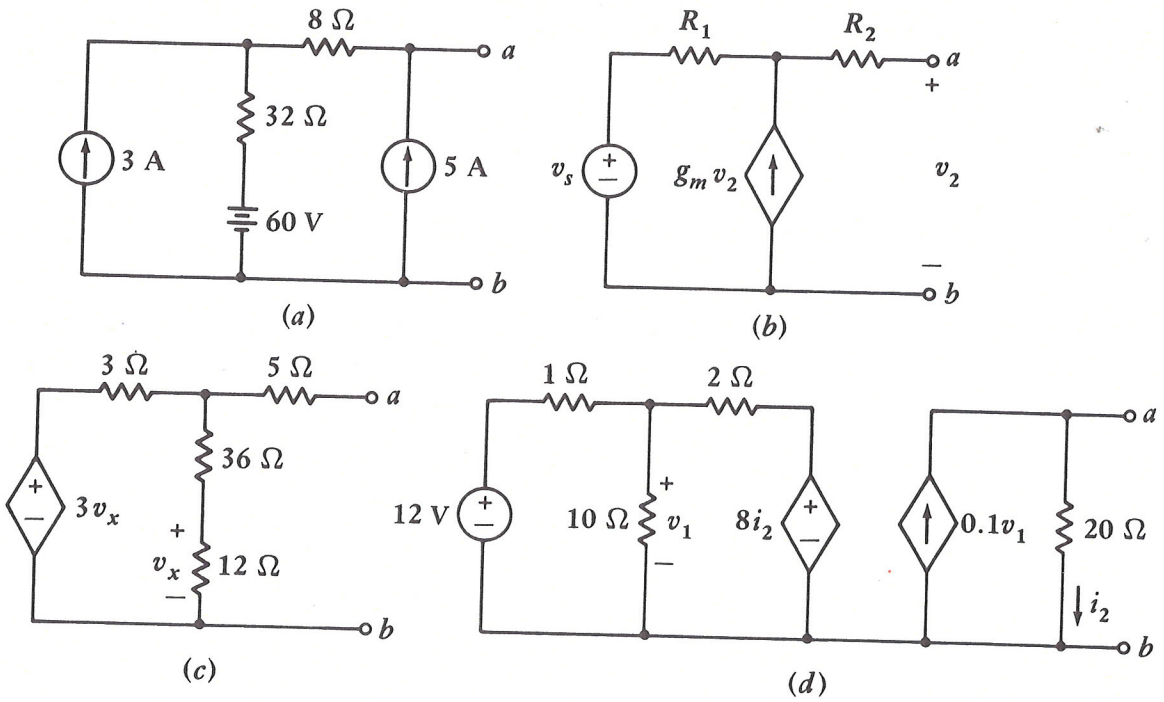


Fig. 3-30: See Drill Probs. 3-8 and 3-9.

3-7 Trees and general nodal analysis

In this section we shall generalize the method of nodal analysis that we have come to know and love. Since nodal analysis is applicable to any network, we cannot promise that we shall be able to solve a wider class of circuit problems. We can, however, look forward to being able to select a general nodal analysis method for any particular problem that may result in fewer equations and less work.

We must first extend our list of definitions relating to network topology. We begin by defining *topology* itself as a branch of geometry which is concerned with those properties of a geometrical figure which are unchanged when the figure is twisted, bent, folded, stretched, squeezed, or tied in knots, with the provision that no parts of the figure are to be cut apart or to be joined together. A sphere and a tetrahedron are topologically identical, as are a square and a circle. In terms of electric circuits, then, we are not now concerned with the particular types of elements appearing in the circuit, but only with the way in which branches and nodes are arranged. As a matter of fact, we usually suppress the nature of the elements and simplify the drawing of the circuit by showing the elements as lines. The resultant drawing is called a *linear graph,* or simply a *graph.* A circuit and its graph are shown in Fig. 3-31. Note that all nodes are identified by heavy dots in the graph.

Since the topological properties of the circuit or its graph are unchanged when it is distorted, the three graphs shown in Fig. 3-32 are all topologically identical with the circuit and graph of Fig. 3-31.

[7] This and the following section may be postponed if desired. They introduce analysis methods that are a little more general than those using node-to-reference voltages and mesh currents. Their use can lead to fewer equations or more useful current and voltage variables.

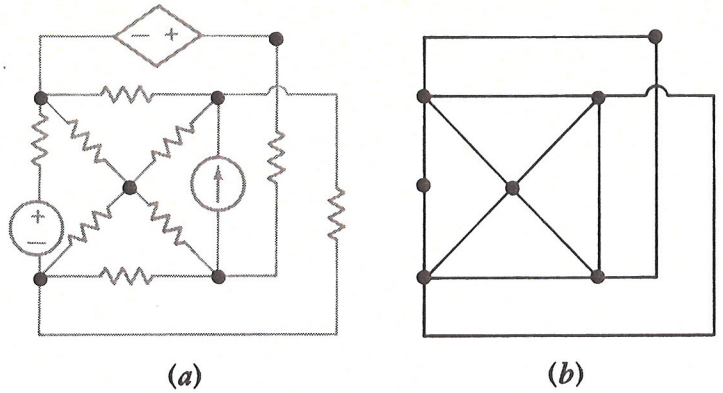


Fig. 3-31: (*a*) A given circuit. (*b*) The linear graph of this circuit.

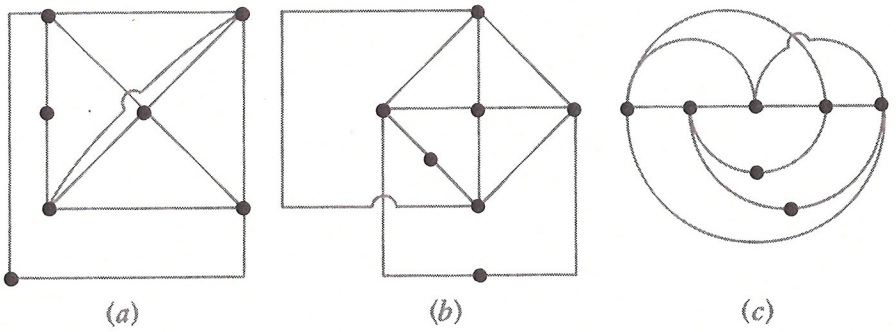


Fig. 3-32: The three graphs shown are topologically identical to each other and to the graph of Fig. 3-31*b*, and each is a graph of the circuit shown in Fig. 3-31a.

Topological terms which we already know and have been using correctly are:

node: a point at which two or more elements have a common connection.
path: a set of elements that may be traversed in order without passing through the same node twice.
branch: a single path, containing one simple element, which connects one node to any other node.
loop: a closed path.
mesh: a loop which does not contain any other loops within it.
planar circuit: a circuit which may be drawn on a plane surface in such a way that no branch passes over or under any other branch.
nonplanar circuit: any circuit which is not planar.

The graphs of Fig. 3-32 each contain 12 branches and 7 nodes.

Three new properties of a linear graph must now be defined, a tree, a cotree, and a link. We define a *tree* as any set of branches which does not contain any loops and yet connects every node to every other node, not necessarily directly. There are usually a number of different trees which may be drawn for a network, and the number increases rapidly as the complexity of the network increases. The simple graph shown in Fig. 3-33*a* has eight possible trees, four of which are shown by heavy lines in Figs. 3-33*b*, *c*, *d*, and *e*.

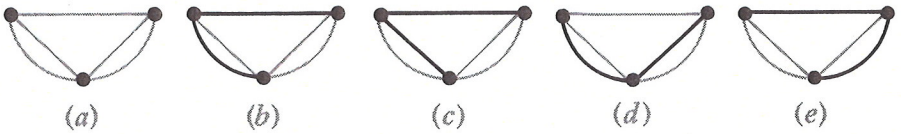


Fig. 3-33: (*a*) The linear graph of a three-node network. (*b*), (*c*), (*d*), and (*e*) Four of the eight different trees which may be drawn for this graph are shown by the heavy lines.

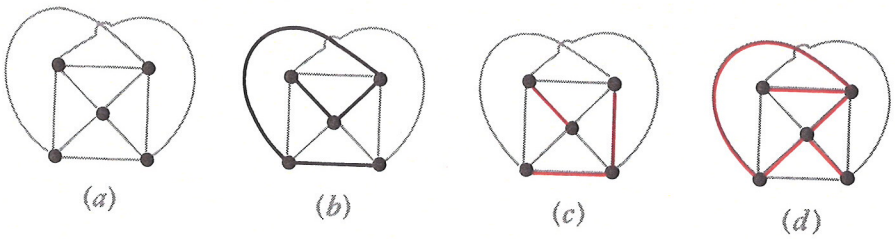


Fig. 3-34: (*a*) A linear graph. (*b*) A possible tree for this graph. (*c*) and (*d*) These sets of branches do not satisfy the definition of a tree.

In Fig. 3-34*a* a more complex graph is shown. Figure 3-34*b* shows one possible tree, and Figs. 3-34*c* and *d* show sets of branches which are *not* trees because neither set satisfies the definition above.

After a tree has been specified, those branches that are not part of the tree form the *cotree*, or complement of the tree. The lightly drawn branches in Figs. 3-33*b* to *e* show the cotrees that correspond to the heavier trees.

Once we understand the construction of a tree and its cotree, the concept of the link is very simple, for a *link* is any branch belonging to the cotree. It is evident that any particular branch may or may not be a link, depending on the particular tree which is selected.

The number of links in a graph may be related to the number of branches and nodes very simply. If the graph has N nodes, then exactly $(N - 1)$ branches are required to construct a tree because the first branch chosen connects two nodes and each additional branch includes one more node. Thus, given B branches, the number of links L must be

$$L = B - (N - 1)$$

or

$$L = B - N + 1 \tag{30}$$

There are L branches in the cotree and $(N - 1)$ branches in the tree.

In any of the graphs shown in Fig. 3-33, we note that $3 = 5 - 3 + 1$, and in the graph of Fig. 3-34*b*, $6 = 10 - 5 + 1$. A network may be in several disconnected parts, and (30) may be made more general by replacing $+1$ with $+S$, where S is the number of separate parts. However, it is also possible to connect two separate parts by a *single* conductor, thus causing two nodes to form one node; no current can flow through this single conductor. This process may be used to join any number of separate parts, and thus we shall not suffer any loss of generality if we restrict our attention to circuits for which $S = 1$.

We are now ready to discuss a method by which we may write a set of nodal equations that are independent and sufficient. The method will enable us to obtain many different sets of equations for the same network, and all the sets will be valid. However, the method does not provide us with *every* possible set of equations. Let us first describe the procedure, illustrate it by three examples, and then point out the reason that the equations are independent and sufficient.

Given a network, we should:

1 Draw a graph and then identify a tree.
2 Place all voltage sources in the tree.
3 Place all current sources in the cotree.

4 Place all control-voltage branches for voltage-controlled dependent sources in the tree, if possible.
5 Place all control-current branches for current-controlled dependent sources in the cotree, if possible.

These last four steps effectively associate voltages with the tree and currents with the cotree.

We now assign a voltage variable (with its plus-minus pair) across each of the $(N - 1)$ branches in the tree. A branch containing a (dependent or independent) voltage source should be assigned that source voltage, and a branch containing a controlling voltage should be assigned that controlling voltage. The number of new variables that we have introduced is therefore equal to the number of branches in the tree $(N - 1)$, reduced by the number of voltage sources in the tree, and reduced also by the number of control voltages we were able to locate in the tree. In the third example below, we shall find that the number of new variables required may be zero.

Having a set of variables, we now need to write a set of equations that are sufficient to determine these variables. The equations are obtained through the application of KCL. Voltage sources are handled in the same way as in our earlier attack on nodal analysis; each voltage source and the two nodes at its terminals comprise a supernode or a part of a supernode. Kirchhoff's current law is then applied at all but one of the remaining nodes and supernodes. We set the sum of the currents leaving the node in all of the branches connected to it equal to zero. Each current is expressed in terms of the voltage variables we just assigned. One node may be ignored, just as was the case earlier for the reference node. Finally, in case there are current-controlled dependent sources, we must write an equation for each control current that relates it to the voltage variables; this also is no different from the procedure used before with nodal analysis.

Let us try out this process on the circuit shown in Fig. 3-35*a*. It contains four nodes and five branches, and its graph is shown in Fig. 3-35*b*. In accor-

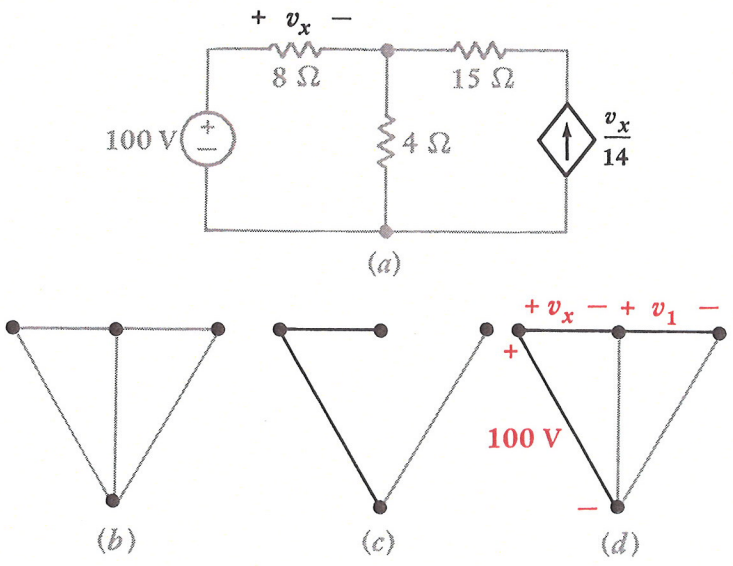


Fig. 3-35: (*a*) A circuit used as an example for general nodal analysis. (*b*) The graph of the given circuit. (*c*) The voltage source and the control voltage are placed in the tree, while the current source goes in the cotree. (*d*) The tree is completed and a voltage is assigned across each tree branch.

dance with steps 2 and 3 of the tree-drawing procedure, we place the voltage source in the tree and the current source in the cotree. Following step 4, we see that the v_x branch may also be placed in the tree since it does not form any loop which would violate the definition of a tree. We have now arrived at the two tree branches and the single link shown in Fig. 3-35*c*, and we see that we do not yet have a tree since the right node is not connected to the others by a path through tree branches. The only possible way to complete the tree is shown in Fig. 3-35*d*. The 100-V source voltage, the control voltage v_x, and a new voltage variable v_1 are next assigned to the three tree branches as shown.

We therefore have two unknowns, v_x and v_1, and it is obvious that we need to obtain two equations in terms of them. There are four nodes, but the presence of the voltage source causes two of them to form a single supernode. Kirchhoff's current law may be applied at any two of the three remaining nodes or supernodes. Let's attack the right node first. The current leaving to the left is $-v_1/15$, while that leaving downward is $-v_x/14$. Thus, our first equation is

$$-\frac{v_1}{15} - \frac{v_x}{14} = 0$$

The central node at the top looks easier than the supernode, so we set the sum of the current to the left, $-v_x/8$, the current to the right, $v_1/15$, and the downward current through the 4-Ω resistor equal to zero. This latter current is given by the voltage across the resistor divided by 4 Ω, but there is no voltage labeled on that link. However, when a tree is constructed according to the definition, there is a path through it from any node to any other node. Then, since every branch in the tree is assigned a voltage, we may express the voltage across any link in terms of the tree-branch voltages. This downward current is therefore $(-v_x + 100)/4$, and we have the second equation,

$$-\frac{v_x}{8} + \frac{v_1}{15} + \frac{-v_x + 100}{4} = 0$$

The simultaneous solution of these two nodal equations gives $v_1 = -60$ V, $v_x = 56$ V.

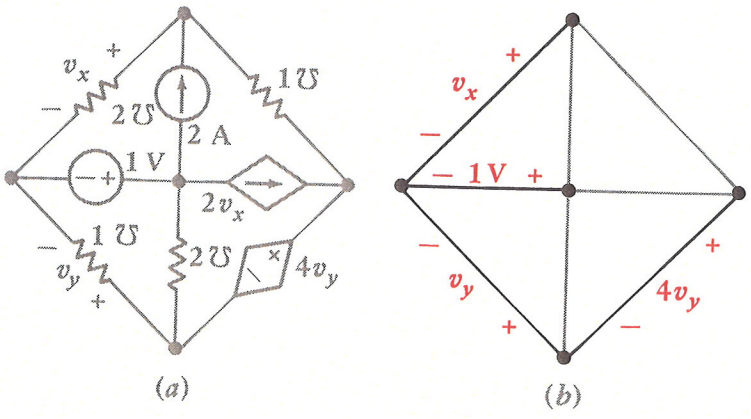


Fig. 3-36: (*a*) The circuit of Fig. 3-5 is repeated. (*b*) A tree is chosen such that both voltage sources and both control voltages are tree branches.

As a second example, let us reconsider a more complex circuit that we first analyzed by defining all node voltages with respect to a reference node. The circuit is that of Fig. 3-5, repeated as Fig. 3-36*a*. We draw a tree so that both voltage sources and both control voltages appear as tree-branch voltages and, hence, as assigned variables. As it happens, these four branches constitute a tree, Fig. 3-36*b*, and tree-branch voltages v_x, 1, v_y, and $4v_y$ are chosen, as shown.

Both voltage sources define supernodes and we apply KCL twice, once to the top node,

$$2v_x + 1(v_x - v_y - 4v_y) = 2$$

and once to the supernode consisting of the right node, the bottom node, and the dependent voltage source,

$$1v_y + 2(v_y - 1) + 1(4v_y + v_y - v_x) = 2v_x$$

Instead of the four equations we had previously, we have only two, and we find easily that $v_x = \frac{26}{9}$ V and $v_y = \frac{4}{3}$ V, both values agreeing with the earlier solution.

For a final example we consider the circuit of Fig. 3-37*a*. The two voltage sources and the control voltage establish the three-branch tree shown in Fig. 3-37*b*. Since the two upper and the lower right node all join to form one supernode, we need write only one KCL equation. Selecting the lower left node, we have

$$-1 - \frac{v_x}{4} + 3 + \frac{-v_x + 30 + 6v_x}{5} = 0$$

and it follows that $v_x = -\frac{32}{3}$ V. In spite of the apparent complexity of this circuit, the use of general nodal analysis has led to an easy solution. Employing mesh currents or node-to-reference voltages would require more equations and more effort.

We shall discuss the problem of finding the best analysis scheme in the following section.

If we should need to know some other voltage, current, or power in the previous example, one additional step would give the answer. For example, the power provided by the 3-A source is $3(-30 - \frac{32}{3}) = -122$ W.

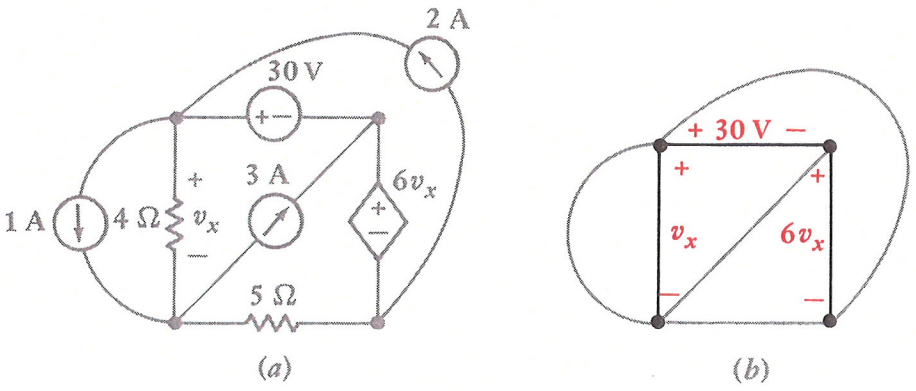


Fig. 3-37: (*a*) A circuit for which only one general nodal equation need be written. (*b*) The tree and the tree-branch voltages used.

Let us conclude by discussing the sufficiency of the assumed set of tree-branch voltages and the independence of the nodal equations. If these tree-branch voltages are *sufficient,* then the voltage of every branch in either the tree or the cotree must be obtainable from a knowledge of the values of all the tree-branch voltages. This is certainly true for those branches in the tree. For the links we know that each link extends between two nodes, and, by definition, the tree must also connect those two nodes. Hence, every link voltage may also be established in terms of the tree-branch voltages.

Once the voltage across every branch in the circuit is known, then all the currents may be found by using either the given value of the current if the branch consists of a current source, Ohm's law if it is a resistive branch, or by using KCL and these current values if the branch happens to be a voltage source. Thus, all the voltages and currents are determined and sufficiency is demonstrated.

To demonstrate independency, let us satisfy ourselves by assuming the situation where the only sources in the network are independent current sources. As we have noticed earlier, independent voltage sources in the circuit result in fewer equations, while dependent sources usually necessitate a greater number of equations. For independent current sources only, there will then be precisely $(N - 1)$ nodal equations written in terms of $(N - 1)$ tree-branch voltages. To show that these $(N - 1)$ equations are *independent,* visualize the application of KCL to the $(N - 1)$ different nodes. Each time we write the KCL equation, there is a new tree branch involved—the one which connects that node to the remainder of the tree. Since that circuit element has not appeared in any previous equation, we must obtain an independent equation. This is true for each of the $(N - 1)$ nodes in turn, and hence we have $(N - 1)$ independent equations.

Drill Problem

3-10. (*a*) How many trees may be constructed for the circuit of Fig. 3-38 that follow all five of the tree-drawing suggestions listed earlier? (*b*) Draw a suitable tree, write two equations in two unknowns, and find v_x. (*c*) What power is supplied by the dependent source? *Ans:* 1; 250 V; 20.5 kW

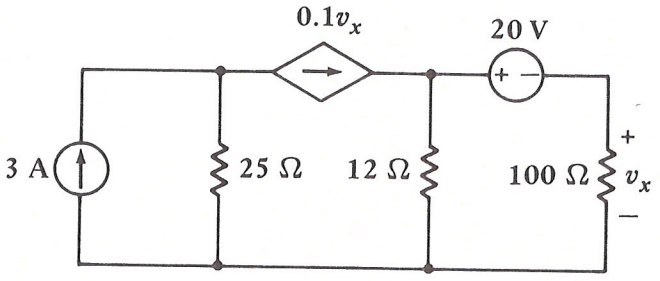


Fig. 3-38: See Drill Prob. 3-10.

3-8 Links and loop analysis

Now we shall consider the use of a tree to obtain a suitable set of loop equations. In some respects this is the dual of the method of writing nodal equations. Again it should be pointed out that, although we are able to guarantee that any set of equations we write will be both sufficient and independent, we should not expect that the method will lead directly to every possible set of equations.

We again begin by constructing a tree, and we use the same set of rules as we did for general nodal analysis. The objective either for nodal or loop analysis is to place voltages in the tree and currents in the cotree; this is a mandatory rule for sources and a desirable rule for controlling quantities.

Now, however, instead of assigning a voltage to each branch in the tree, we assign a current (including reference arrow, of course) to each element in the cotree or to each link. If there were ten links, we would assign exactly 10 link currents. Any link that contains a current source is assigned that source current as the link current. Note that each link current may also be thought of as a loop current, for the link must extend between two specific nodes, and there must also be a path between those same two nodes through the tree. Thus, with each link there is associated a single loop that includes that one link and a unique path through the tree. It is evident that the assigned current may be thought of either as a loop current or as a link current. The link connotation is most helpful at the time the currents are being defined, for one must be established for each link; the loop interpretation is more convenient at equation-writing time, because we shall apply KVL around each loop.

Let us try out this process of defining link currents by reconsidering an earlier example we worked using mesh currents. The circuit is shown in Fig. 3-12 and redrawn in Fig. 3-39*a*. The tree selected is one of several that might be constructed for which the voltage source is in a tree branch and the current source is in a link. Let us first consider the link containing the current source. The loop associated with this link is the left-hand mesh, so we show our link current flowing about the perimeter of this mesh, Fig. 3-39*b*. An obvious choice for the symbol for this link current is "7 A." Remember that no other current can flow through this particular link, and thus its value must be exactly the strength of the current source.

We next turn our attention to the 3-Ω resistor link. The loop associated with it is the upper right-hand mesh, and this loop (or mesh) current is defined as i_A and also shown in Fig. 3-39*b*. The last link is the lower 1-Ω resistor, and the only path between its terminals through the tree is around the perimeter of the circuit. That link current is called i_B, and the arrow indicating its path and reference direction appears in Fig. 3-39*b*. It is not a mesh current.

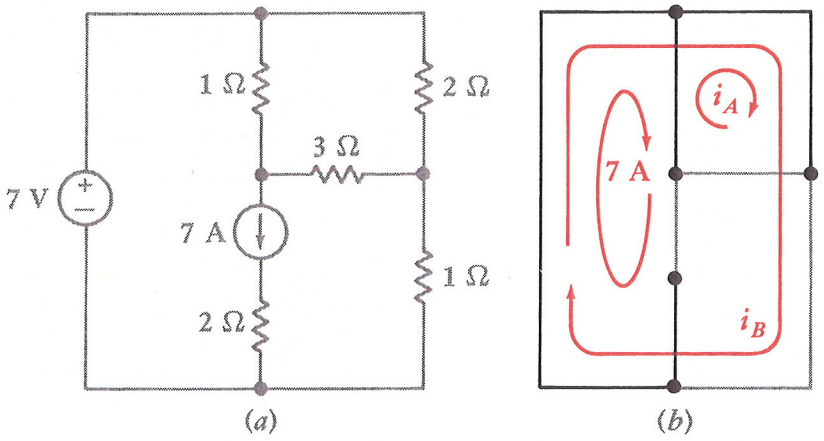


Fig. 3-39: (*a*) The circuit of Fig. 3-12 is shown again. (*b*) A tree is chosen such that the current source is in a link and the voltage source is in a tree branch.

Note that each link has only one current present in it, but a tree branch may have any number from one to the total number of link currents assigned. The use of long, almost closed, arrows to indicate the loops helps to indicate which loop currents flow through which tree branch and what their reference directions are.

A KVL equation must now be written around each of these loops. The variables used are the assigned link currents. Since the voltage across a current source cannot be expressed in terms of the source current, and since we have already used the value of the source current as the link current, we discard any loop containing a current source.

For the example of Fig. 3-39, we first traverse the i_A loop, proceeding clockwise from its lower left corner. The current going our way in the 1-Ω resistor is $(i_A - 7)$, in the 2-Ω element it is $(i_A + i_B)$, and in the link it is simply i_A. Thus

$$1(i_A - 7) + 2(i_A + i_B) + 3i_A = 0$$

For the i_B link, clockwise travel from the lower left corner leads to

$$-7 + 2(i_A + i_B) + 1i_B = 0$$

Traversal of the loop defined by the 7-A link is not required. Solving, we have $i_A = 0.5$ A, $i_B = 2$ A, once again. The solution has been achieved with one less equation than before.

An example containing a dependent source appears in Fig. 3-40*a*. This circuit contains six nodes, and its tree therefore must have five branches. Since there are eight elements in the network, there are three links in the

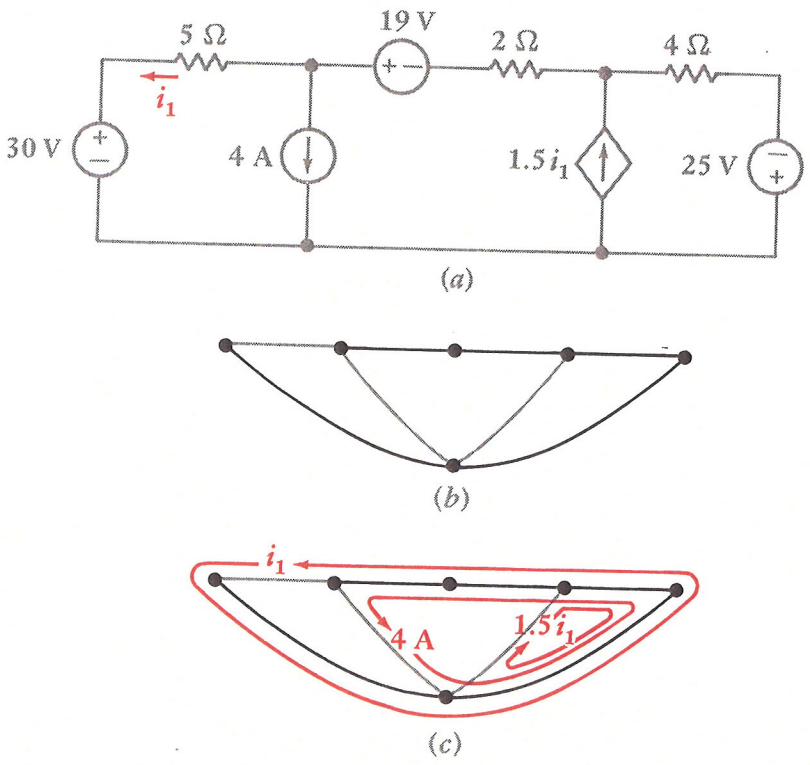


Fig. 3-40: (*a*) A circuit for which i_1 may be found with one equation using general loop analysis. (*b*) The only tree that satisfies the rules outlined in Sec. 3-7. (*c*) The three link currents are shown with their loops.

cotree. If we place the three voltage sources in the tree and the two current sources and the current control in the cotree, we are led to the tree shown in Fig. 3-40*b*. The source current of 4 A defines a loop as shown in Fig. 3-40*c*. The dependent source establishes the loop current $1.5i_1$ around the right mesh, and the control current i_1 gives us the remaining loop current about the perimeter of the circuit. Note that all three currents flow through the 4-Ω resistor.

We have only one unknown quantity, i_1, and, after discarding the loops defined by the two current sources, we apply KVL around the outside of the circuit:

$$-30 + 5(-i_1) + 19 + 2(-i_1 - 4) + 4(-i_1 - 4 + 1.5i_1) - 25 = 0$$

Besides the three voltage sources, there are three resistors in this loop. The 5-Ω resistor has one loop current in it since it is also a link, the 2-Ω resistor contains two loop currents, and the 4-Ω resistor has three. A carefully drawn set of loop currents is a necessity if errors in skipping currents, utilizing extra ones, or erring in the correct direction are to be avoided. The foregoing equation is guaranteed, however, and it leads to $i_1 = -12$ A.

How may we demonstrate sufficiency? Let us visualize a tree. It contains no loops and therefore contains at least two nodes to each of which only one tree branch is connected. The current in each of these two branches is easily found from the known link currents by applying KCL. If there are other nodes at which only one tree branch is connected, these tree-branch currents may also be immediately obtained. In the tree shown in Fig. 3-41, we thus have found the currents in branches *a*, *b*, *c*, and *d*. Now we move along the branches of the tree, finding the currents in the tree branches *e* and *f*; the process may be continued until all the branch currents are determined. The link currents are therefore sufficient to determine all branch currents. It is helpful to look at the situation where an incorrect "tree" has been drawn which contains a loop. Even if all the link currents were zero, a current might still circulate about this "tree loop." Hence, the link currents could not determine this current, and they would not represent a sufficient set. Such a "tree" is by definition impossible.

To demonstrate independence, let us satisfy ourselves by assuming the situation where the only sources in the network are independent voltage sources. As we have noticed earlier, independent current sources in the circuit result in fewer equations, while dependent sources usually necessi-

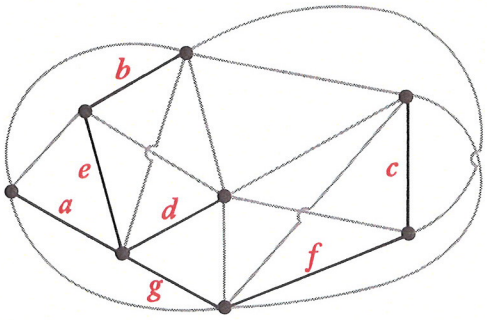


Fig. 3-41: A tree which is used as an example to illustrate the sufficiency of the link currents.

tate a greater number of equations. For independent voltage sources only, there will then be precisely $(B - N + 1)$ loop equations written in terms of the $(B - N + 1)$ link currents. To show that these $(B - N + 1)$ loop equations are independent, it is only necessary to point out that each represents the application of KVL around a loop which contains one link not appearing in any other equation. We might visualize a different resistance $R_1, R_2, \ldots, R_{B-N+1}$ in each of these links, and it is then apparent that one equation can never be obtained from the others since it contains one coefficient not appearing in any other equation.

Hence, the link currents are sufficient to enable a complete solution to be obtained, and the set of loop equations which we use to find the link currents is a set of independent equations.

Having looked at both general nodal analysis and loop analysis, we should now consider the advantages and disadvantages of each method so that an intelligent choice of a plan of attack can be made.

The nodal method in general requires $(N - 1)$ equations, but this number is reduced by one for each independent or dependent voltage source in a tree branch, and increased by one for each dependent source that is voltage controlled by a link voltage or current controlled.

The loop method basically involves $(B - N + 1)$ equations. However, each independent or dependent current source in a link reduces this number by one, while each dependent source that is current controlled by a tree-branch current or is voltage controlled increases the number by one.

As a grand finale for this discussion, let us inspect the T-equivalent-circuit model for a transistor, shown in Fig. 3-42, to which are connected a sinusoidal source, 4 sin 1000t mV, and a 10-kΩ load. We select typical values for the emitter resistance, $r_e = 50\ \Omega$; for the base resistance, $r_b = 500\ \Omega$; for the collector resistance, $r_c = 20\ \text{k}\Omega$; and for the common-base forward-current-transfer ratio, $\alpha = 0.98$. Suppose that we wish to find the input (emitter) current i_e and the load voltage v_L.

Although the details are requested in Drill Probs. 3-12 and 3-13 below, we should see readily that the analysis of this circuit might be accomplished by drawing trees requiring three general nodal equations $(N - 1 - 1 + 1)$ or two loop equations $(B - N + 1 - 1)$. We might also note that three equations are required in terms of node-to-reference voltages, as are three mesh equations.

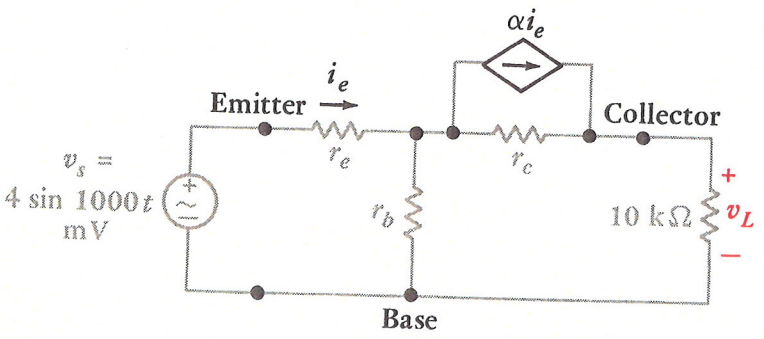


Fig. 3-42: A sinusoidal voltage source and a 10-kΩ load are connected to the T-equivalent circuit of a transistor. The common connection between the input and output is at the base terminal of the transistor and the arrangement is called the common-base configuration.

No matter which method we choose, these results are obtained for this specific circuit:

$$i_e = 18.14 \sin 1000t \quad \mu A$$

$$v_L = 119.6 \sin 1000t \quad mV$$

and we therefore find that this transistor circuit provides a voltage gain (v_L/v_s) of 29.9, a current gain ($v_L/10\,000 i_e$) of 0.659, and a power gain equal to the product, 29.9 (0.659) = 19.70. Higher gains could be secured by operating this transistor in a common-emitter configuration, as illustrated by the equivalent circuit of Prob. 42.

Drill Problems

3-11. Draw a suitable tree and use general loop analysis to find i_A in the circuit of: (*a*) Fig. 3-43*a* by writing just one equation with i_A as the variable; (*b*) Fig. 3-43*b* by writing just two equations with i_A and i_B as the variables.

Ans: 1.6; 9.39 A

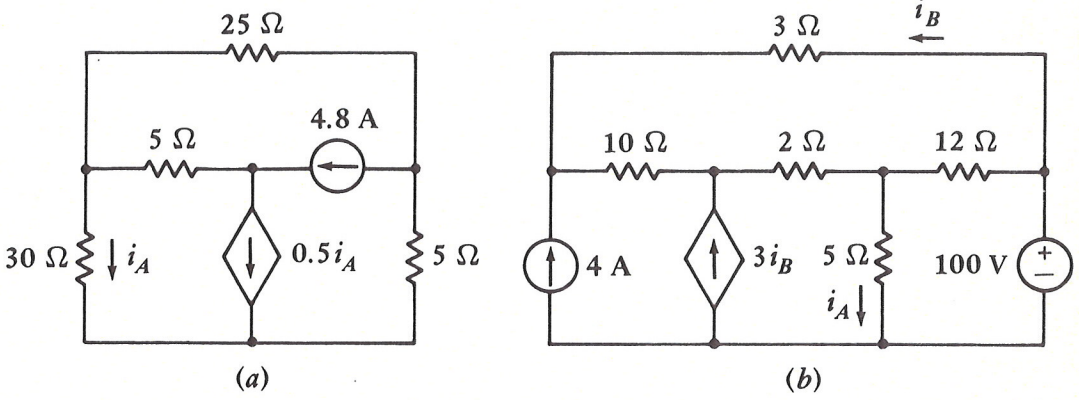
3-12. For the transistor amplifier equivalent circuit shown in Fig. 3-42, let $r_e = 50\,\Omega$, $r_b = 500\,\Omega$, $r_c = 20\,k\Omega$, $\alpha = 0.98$, and find both i_e and v_L by drawing a suitable tree and using: (*a*) two loop equations; (*b*) three nodal equations with a common reference node for the voltages; (*c*) three nodal equations without a common reference node.

Ans: 18.14 sin 1000*t* *m*A; 119.6 sin 1000*t* mV

3-13. Determine the Thévenin and Norton equivalent circuits presented to the 10-kΩ load in Fig. 3-42 by finding: (*a*) the open-circuit value of v_L; (*b*) the (downward) short-circuit current; (*c*) the Thévenin equivalent resistance. All circuit values are given in Drill Prob. 3-12.

Ans: 146.2 sin 1000*t* mV; 65.6 sin 1000*t* μA; 2.23 kΩ

Fig. 3-43: See Drill Prob. 3-11.



Problems

1 (*a*) Find v_2 if $v_1 + 2v_2 + 3v_3 = 20$, $v_1 - 7v_2 - 5v_3 = -5$, and $v_3 + 3v_2 + 4v_1 - 10 = 0$. (*b*) Evaluate the determinant:

$$\begin{vmatrix} 1 & 2 & 3 & 4 \\ 2 & 3 & 4 & 1 \\ 3 & 4 & 1 & -2 \\ 4 & -1 & 2 & 3 \end{vmatrix}$$

2 Use nodal analysis to find v_P in the circuit shown in Fig. 3-44.

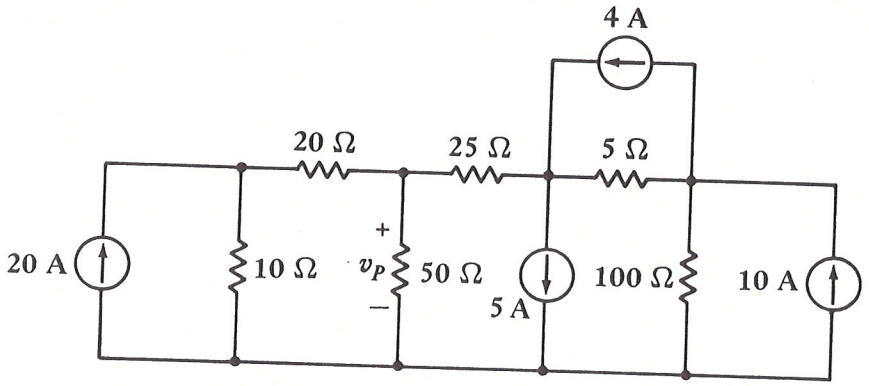


Fig. 3-44: See Prob. 2.

3 Use nodal analysis on the circuit given in Fig. 3-45 to find: (*a*) v_3; (*b*) the power being supplied by the 5-A source.

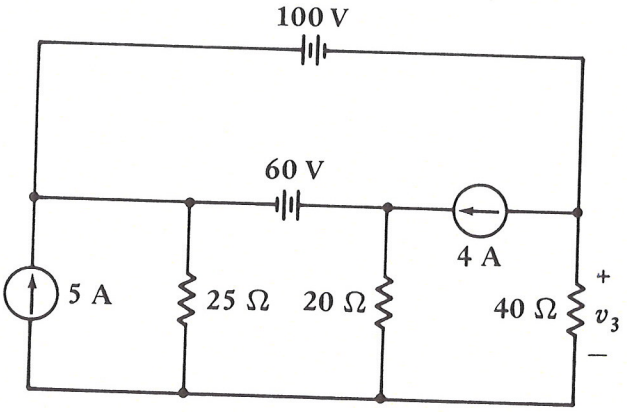


Fig. 3-45: See Prob. 3.

4 Make use of nodal analysis to find v_x and the power delivered to the 50-Ω resistor in the circuit of Fig. 3-46.

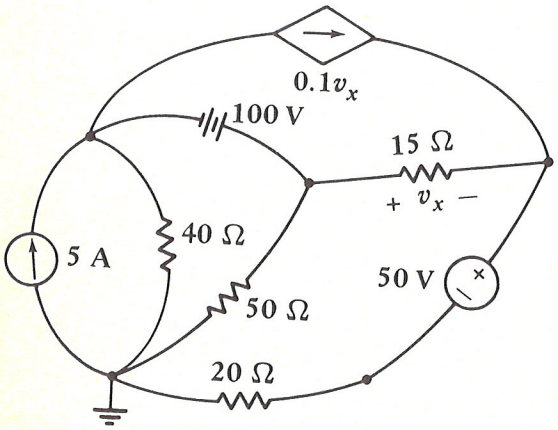


Fig. 3-46: See Prob. 4.

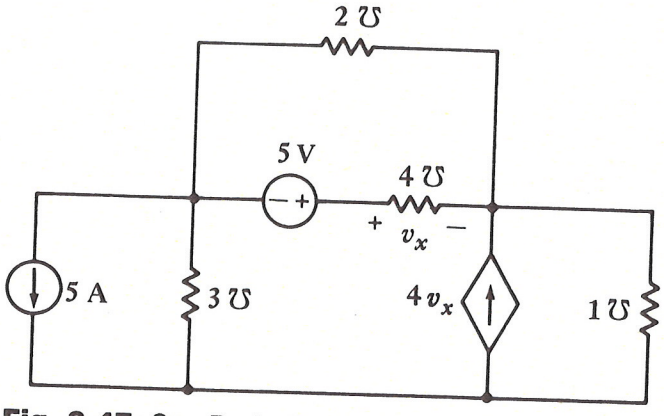


Fig. 3-47: See Prob. 5.

5 Set up nodal equations for the circuit illustrated in Fig. 3-47, and then find the power supplied by the 5-V source.

6 Use nodal analysis to find v_x in the circuit of Fig. 3-48.

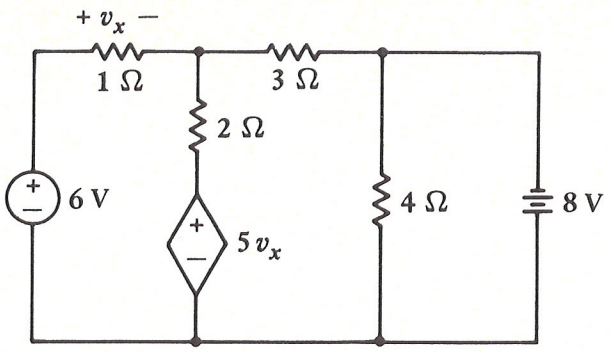


Fig. 3-48: See Probs. 6, 12, and 28.

7 Analyze the circuit of Fig. 3-49 using node voltages and find the power being supplied by the 6-A source.

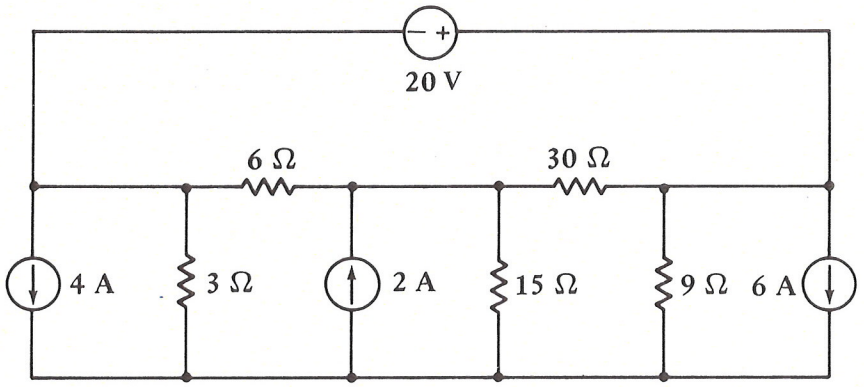


Fig. 3-49: See Prob. 7.

8 In Fig. 3-50, find v_2 through the use of nodal analysis.

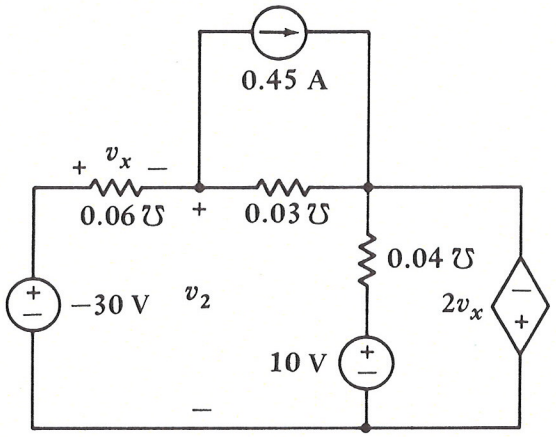


Fig. 3-50: See Prob. 8.

9 In the circuit of Fig. 3-51, use mesh analysis to: (*a*) find the power delivered to the 4-Ω resistor. (*b*) To what voltage should the 100-V battery be changed so that no power is delivered to the 4-Ω resistor?

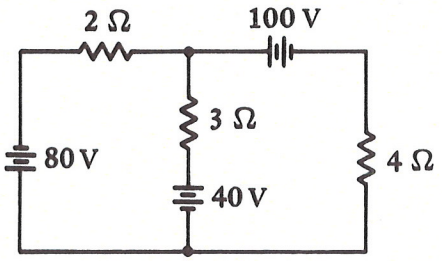


Fig. 3-51: See Prob. 9.

10 Use mesh analysis on the circuit shown in Fig. 3-52 to find the power supplied by the 4-V battery.

11 In Fig. 3-53, every resistance is 6 Ω and every battery voltage is 12 V. Find i_A.

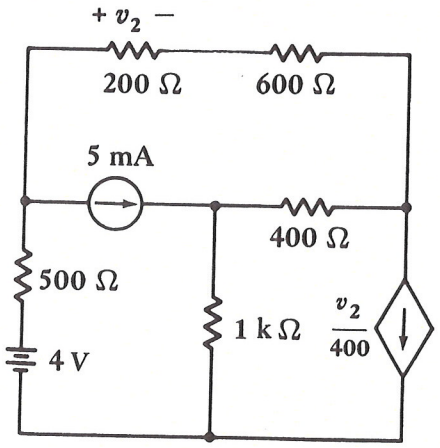


Fig. 3-52: See Prob. 10.

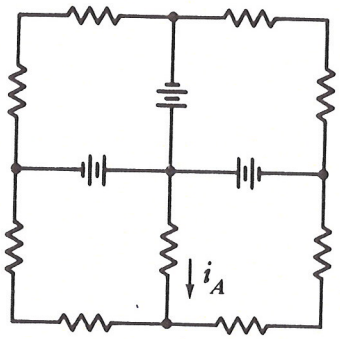


Fig. 3-53: See Prob. 11.

12 In the circuit of Fig. 3-48, change the right-hand element to an 8-A independent current source, arrow directed upward, and use mesh analysis to find the power absorbed by the 3-Ω resistor.

13 Use mesh analysis on the circuit of Fig. 3-54 to find the values of all the mesh currents.

14 In the circuit of Fig. 3-4*b*, use mesh analysis to find i_o, the current flowing downward in R_L if $v_2 = 1.234\,321$ V.

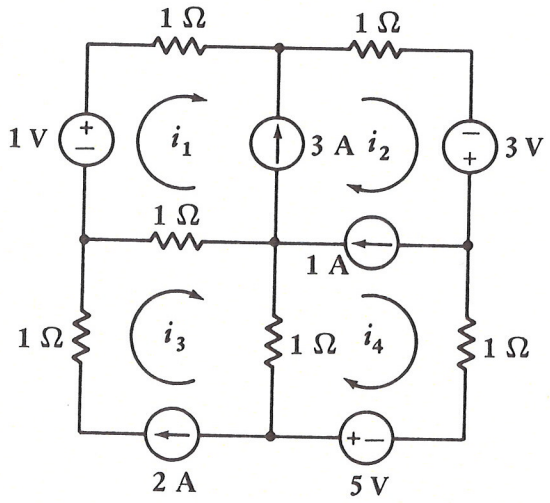


Fig. 3-54: See Prob. 13.

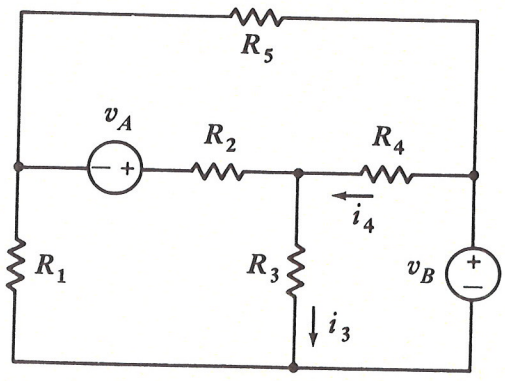


Fig. 3-55: See Prob. 15.