Engineering Circuit Analysis

Fourth Edition

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33 (*a*) Use voltage division, current division, and resistance combination to find i_y in the circuit of Fig. 2-52. (*b*) To what value should the 3-Ω resistance be changed to make $i_y = 1$ A?

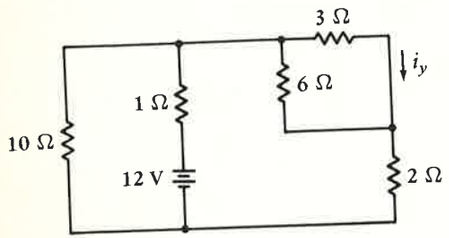


Fig. 2-52: See Prob. 33.

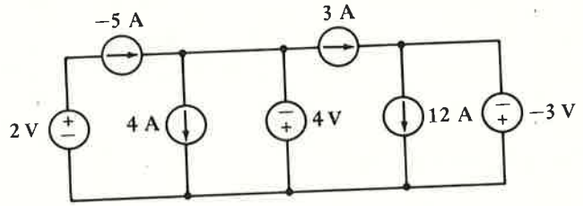


Fig. 2-53: See Prob. 34.

34 The circuit shown in Fig. 2-53 shows several examples of independent current and voltage sources in series and parallel. (*a*) Find the power absorbed by each source. (*b*) To what value should the 4-V source be changed to reduce the power supplied by the −5-A source to zero?

35 A certain op-amp has a gain A of 20 000 and a resistance, $R_i = 50$ kΩ, inside the op-amp between the inverting and noninverting inputs. The op-amp is connected as a voltage follower with $v_s = 1$ V. Find: (*a*) v_o; (*b*) v_i; (*c*) the power supplied by v_s.

36 (*a*) Find v_o for the voltage follower shown in Fig. 2-54*a* if A is large. (*b*) The network shown in Fig. 2-54*b* is connected to the follower output. Find v_x.

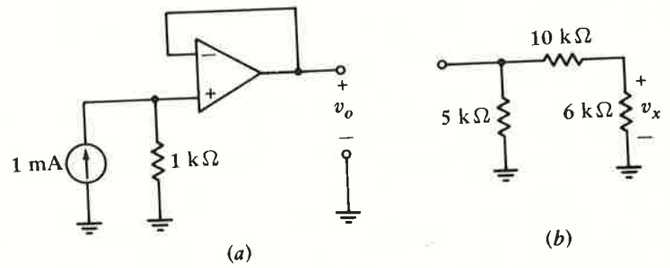


Fig. 2-54: See Prob. 36.

37 (*a*) Find v_x for the circuit shown in Fig. 2-55 if A is large. (*b*) If the op-amp is removed from the circuit and points a and b are connected together, what is v_x?

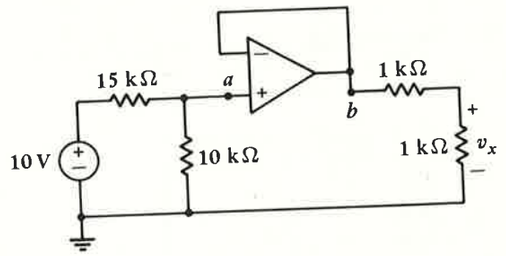


Fig. 2-55: See Prob. 37.

Chapter 3
Some Useful Techniques of Circuit Analysis

3-1 Introduction

We should now be familiar with Ohm's law and Kirchhoff's laws and their application in the analysis of simple series and parallel resistive circuits. When it will produce results more easily we should be able to combine resistors or sources in series or parallel and be able to use the principles of voltage and current division. Most of the circuits on which we have been practicing are simple and of questionable practical importance; they are useful in helping us learn to apply the fundamental laws. Now we must begin analyzing more complicated circuits.

Physical systems which we shall want to analyze and design in the coming years will include electric and electronic control circuits, communication systems, energy converters such as motors and generators, power distribution systems, interconnecting circuits for commercially available integrated circuits, and entertainment or other devices which are now unknown. Many of us will be confronted with allied problems involving heat flow, fluid flow, and the behavior of various mechanical systems. In the analysis of any of these cases it is often helpful to replace the system with an equivalent electric circuit. As an example, we might consider a transistor amplifier, an electronic device which is part of many communication systems and control circuits. Transistors, along with resistors and other passive circuit elements, are used to amplify or magnify electrical signals (voltages or currents) and to direct the amplified signals to desired loads. They are also widely used as components of the high-speed electrical switches and logic circuits that make up the digital computers that pervade our technological society. It is possible to replace the transistor, the resistors, the other passive circuit elements, the signal source, and the load by combinations of simple circuit elements, such as current sources, voltage sources, and resistors. The problem solutions are then achieved by circuit analysis methods which we either know already or will meet in this chapter.

When we are able to describe mathematically the behavior of fluid-flow

and heat-flow systems, the dynamic response of aircraft control surfaces, and other nonelectrical phenomena, we shall see that the resultant equations are often precisely analogous to those describing current and voltage relationships in electric circuits. We may decide, then, that it is much easier and cheaper to construct the analogous electric circuit than it is to build a prototype of the actual physical system. The electric circuit may then be used to predict the performance of the other system as various elements are changed and may help achieve a better final design. This is the basis on which the electronic analog computer operates.

It is evident that one of the primary goals of this chapter must be learning methods of simplifying the analysis of more complicated circuits. Among these methods will be superposition, loop, mesh, and nodal analysis. We shall also try to develop the ability to select the most convenient analysis method. Most often we are interested only in the detailed performance of an isolated portion of a complex circuit; a method of replacing the remainder of the circuit by a greatly simplified equivalent is then very desirable. The equivalent is often a single resistor in series or parallel with an ideal source. Thévenin's and Norton's theorems will enable us to effect this replacement.

We shall begin studying methods of simplifying circuit analysis by considering a powerful general method, that of nodal analysis.

3-2 Nodal analysis

In the previous chapter we considered the analysis of a simple circuit containing only two nodes. We found then that the major step of the analysis was taken as we obtained a single equation in terms of a single unknown quantity, the voltage between the pair of nodes. We shall now let the number of nodes increase, and correspondingly provide one additional unknown quantity and one additional equation for each added node. Thus, a three-node circuit should have two unknown voltages and two equations; a ten-node circuit will have nine unknown voltages and nine equations; and an N-node circuit will need $(N-1)$ voltages and $(N-1)$ equations.

We consider the mechanics of nodal analysis in this section, but the justification for our methods will not be developed until later in this chapter.

As an example, let us consider the three-node circuit shown in Fig. 3-1*a*. We may emphasize the locations of the three nodes by redrawing the circuit, as shown in Fig. 3-1*b*, where each node is identified by a number. We would now like to associate a voltage with each node, but we must remember that a voltage must be defined as existing between *two nodes* in a network. We thus select one node as a reference node, and then define a voltage between each remaining node and the reference node. Hence, we note again that there will be only $(N-1)$ voltages defined in an N-node circuit.

We choose node 3 as the reference node. Either of the other nodes could have been selected, but a little simplification in the resultant equations is obtained if the node to which the greatest number of branches is connected is identified as the reference node. If there is a ground node, it is usually most convenient to select it as the reference node. More often than not, the ground node appears as a common lead across the bottom of a circuit diagram.

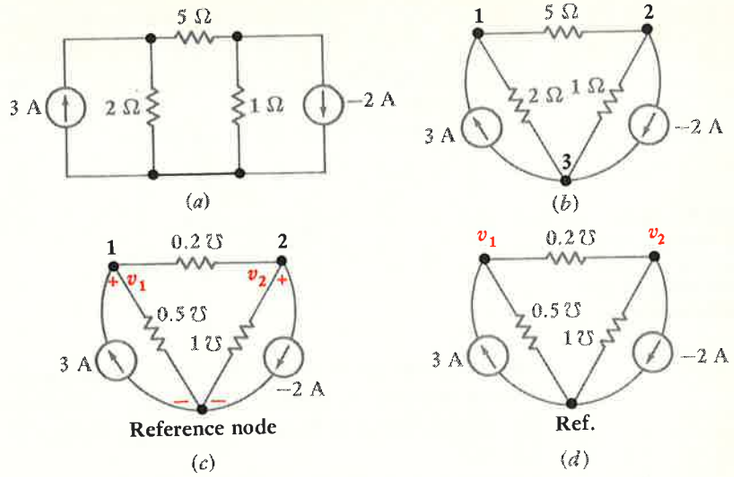


Fig. 3-1: (*a*) A given three-node circuit. (*b*) The circuit is redrawn to emphasize the three nodes, and each node is numbered. (*c*) A voltage, including polarity reference, is assigned between each node and the reference node. (*d*) The voltage assignment is simplified by eliminating the polarity references; it is understood that each voltage is sensed positive relative to the reference node.

The voltage of node 1 relative to the reference node 3 is defined as v_1, and v_2 is defined as the voltage of node 2 with respect to the reference node. These two voltages are sufficient, and the voltage between any other pair of nodes may be found in terms of them. For example, the voltage of node 1 with respect to node 2 is $(v_1 - v_2)$. The voltages v_1 and v_2 and their reference signs are shown in Fig. 3-1*c*. In this figure the resistance values have also been replaced with conductance values.

The circuit diagram is finally simplified in Fig. 3-1*d* by eliminating all voltage reference symbols. A reference node is plainly marked, and the voltage placed at each remaining node is *understood* to be the voltage of that node with respect to the reference node. This is the only situation for which we should use voltage symbols without the associated plus-minus-sign pair, except for the battery symbol that was defined in Fig. 1-14*b*.

We must now apply Kirchhoff's current law to nodes 1 and 2. We do this by equating the total current leaving the node through the several conductances to the total source current entering the node. Thus,

$$0.5v_1 + 0.2(v_1 - v_2) = 3$$

or

$$0.7v_1 - 0.2v_2 = 3 \tag{1}$$

At node 2 we obtain

$$1v_2 + 0.2(v_2 - v_1) = 2$$

or

$$-0.2v_1 + 1.2v_2 = 2 \tag{2}$$

Equations (1) and (2) are the desired two equations in two unknowns, and they may be solved easily. The results are:

$$v_1 = 5 \quad \text{V}$$

$$v_2 = 2.5 \quad \text{V}$$

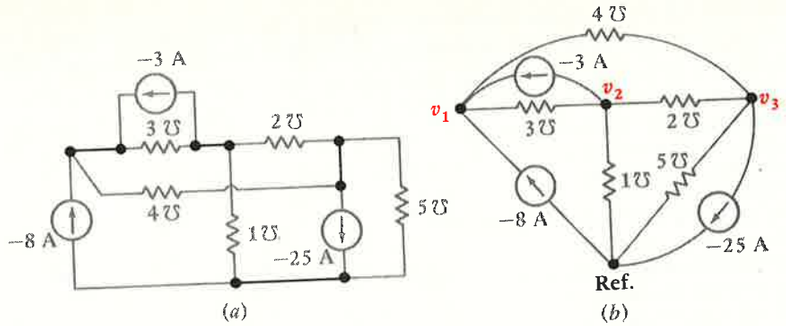


Fig. 3-2: (*a*) A circuit containing four nodes and eight branches. (*b*) The same circuit redrawn with node voltages assigned.

Also, the voltage of node 1 relative to node 2 is $(v_1 - v_2)$, or 2.5 V, and any current or power in the circuit may now be found in one step. For example, the current directed downward through the 0.5-Ʊ conductance is $0.5v_1$, or 2.5 A.

Now let us increase the number of nodes by one. A new circuit is shown in Fig. 3-2*a*, and it is redrawn in Fig. 3-2*b*, with the nodes identified, a convenient reference node chosen, and the node voltages specified. We next sum the currents leaving node 1:

$$3(v_1 - v_2) + 4(v_1 - v_3) - (-8) - (-3) = 0$$

or

$$7v_1 - 3v_2 - 4v_3 = -11 \tag{3}$$

At node 2:

$$3(v_2 - v_1) + 1v_2 + 2(v_2 - v_3) - 3 = 0$$

or

$$-3v_1 + 6v_2 - 2v_3 = 3 \tag{4}$$

and at node 3:

$$4(v_3 - v_1) + 2(v_3 - v_2) + 5v_3 - 25 = 0$$

or

$$-4v_1 - 2v_2 + 11v_3 = 25 \tag{5}$$

Equations (3) through (5) may be solved by a simple process of elimination of variables, or by Cramer's rule and determinants.[1] Using the latter method, we have

$$v_1 = \frac{\begin{vmatrix} -11 & -3 & -4 \\ 3 & 6 & -2 \\ 25 & -2 & 11 \end{vmatrix}}{\begin{vmatrix} 7 & -3 & -4 \\ -3 & 6 & -2 \\ -4 & -2 & 11 \end{vmatrix}}$$

[1] Appendix 1 provides a short review of determinants and the solution of a system of simultaneous linear equations by Cramer's rule.

Expanding the numerator and denominator determinants by minors along their first columns leads to

$$v_1 = \frac{-11\begin{vmatrix} 6 & -2 \\ -2 & 11 \end{vmatrix} - 3\begin{vmatrix} -3 & -4 \\ -2 & 11 \end{vmatrix} + 25\begin{vmatrix} -3 & -4 \\ 6 & -2 \end{vmatrix}}{7\begin{vmatrix} 6 & -2 \\ -2 & 11 \end{vmatrix} - (-3)\begin{vmatrix} -3 & -4 \\ -2 & 11 \end{vmatrix} + (-4)\begin{vmatrix} -3 & -4 \\ 6 & -2 \end{vmatrix}}$$

$$= \frac{-11(62) - 3(-41) + 25(30)}{7(62) + 3(-41) - 4(30)} = \frac{-682 + 123 + 750}{434 - 123 - 120}$$

$$= \frac{191}{191} = 1 \quad \text{V}$$

Similarly,

$$v_2 = \frac{\begin{vmatrix} 7 & -11 & -4 \\ -3 & 3 & -2 \\ -4 & 25 & 11 \end{vmatrix}}{191} = 2 \quad \text{V}$$

and

$$v_3 = \frac{\begin{vmatrix} 7 & -3 & -11 \\ -3 & 6 & 3 \\ -4 & -2 & 25 \end{vmatrix}}{191} = 3 \quad \text{V}$$

The denominator determinant is common to each of the three evaluations above. For circuits that do not contain either voltage sources or dependent sources (i.e., circuits containing only independent current sources), this denominator is the determinant of a matrix[2] that is defined as the *conductance matrix* of the circuit:

$$\mathbf{G} = \begin{bmatrix} 7 & -3 & -4 \\ -3 & 6 & -2 \\ -4 & -2 & 11 \end{bmatrix}$$

It should be noted that the nine elements of the matrix are the ordered array of the coefficients of Eqs. (3), (4), and (5), each of which is a conductance value. The first row is composed of the coefficients of the KCL equation at the first node, the coefficients being given in the order of v_1, v_2, and v_3. The second row applies to the second node, and so on.

The conductance matrix is symmetrical about the major diagonal (upper left to lower right), and all elements not on this diagonal are negative, whereas all elements on it are positive. This is a general consequence of the systematic way in which we assigned variables, applied KCL, and ordered the equations, as well as of the reciprocity theorem, which we shall discuss

[2] We shall not begin to manipulate matrices mathematically until Chap. 16; at that time a rudimentary knowledge of linear algebra is presumed.

in Chap. 16. For the present, we merely acknowledge the symmetry in these circuits that have only independent current sources and accept the check that it provides us in discovering errors we may have committed in writing circuit equations.

We still must see how voltage sources and dependent sources affect the strategy of nodal analysis. We now investigate the consequences of including a voltage source.

As a typical example, consider the circuit shown in Fig. 3-3. Our previous four-node circuit has been changed by replacing the 2-℧ conductance between nodes 2 and 3 by a 22-V voltage source. We still assign the same node-to-reference voltages, v_1, v_2, and v_3. Previously, the next step was the application of KCL at each of the three nonreference nodes. If we try to do that once again, we see that we shall run into some difficulty at both nodes 2 and 3, for we do not know what the *current* is in the branch with the *voltage* source. There is no way by which we can express the current as a function of the voltage, for the definition of a voltage source is exactly that the voltage is independent of the current.

There are two ways out of these difficulties. The more difficult is to assign an unknown current to the branch with the voltage source, proceed to apply KCL three times, and then apply KVL once between nodes 2 and 3; the result is four equations in four unknowns for this example.

The easier method is to agree that we are primarily interested in the node voltages, so that we may avoid the current in the voltage-source branch that is causing our problems. We do this by treating node 2, node 3, and the voltage source together as a sort of supernode and applying KCL to both nodes at the same time. This is certainly possible, because, if the total current leaving node 2 is zero and the total current leaving node 3 is zero, then the total current leaving the totality of the two nodes is zero.

The supernode is indicated by the shaded region enclosed by the broken line in Fig. 3-3, and we shall set the sum of the six currents leaving the supernode equal to zero. Beginning with the 3-℧ conductance branch and working clockwise, we have

$$3(v_2 - v_1) - 3 + 4(v_3 - v_1) - 25 + 5v_3 + 1v_2 = 0$$

or

$$-7v_1 + 4v_2 + 9v_3 = 28$$

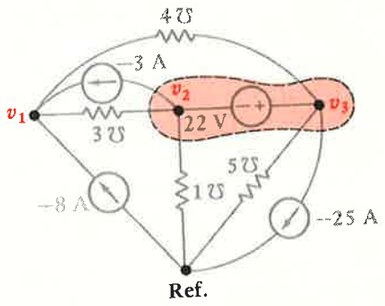


Fig. 3-3: The 2-℧ conductance in the circuit of Fig. 3-2 is replaced by an independent voltage source. Kirchhoff's current law is used on the supernode enclosed by the broken line, and the source voltage is set equal to $v_3 - v_2$.

The KCL equation at node 1 is unchanged from (3):

$$7v_1 - 3v_2 - 4v_3 = -11$$

We need one additional equation since we have three unknowns, and it must utilize the fact that there is a 22-V voltage source between nodes 2 and 3,

$$v_3 - v_2 = 22$$

Rewriting these last three equations,

$$7v_1 - 3v_2 - 4v_3 = -11$$

$$-7v_1 + 4v_2 + 9v_3 = 28$$

$$-v_2 + v_3 = 22$$

the determinant solution for v_1 is

$$v_1 = \frac{\begin{vmatrix} -11 & -3 & -4 \\ 28 & 4 & 9 \\ 22 & -1 & 1 \end{vmatrix}}{\begin{vmatrix} 7 & -3 & -4 \\ -7 & 4 & 9 \\ 0 & -1 & 1 \end{vmatrix}} = \frac{-189}{42} = -4.5 \quad \text{V}$$

Note the lack of symmetry about the major diagonal in the denominator determinant as well as the fact that not all of the off-diagonal elements are negative. This is the result of the presence of the voltage source. Note also that it would not make much sense to call the denominator the determinant of the *conductance* matrix, because the bottom row comes from the equation $-v_2 + v_3 = 22$, and this equation does not depend on conductances in any way.

The presence of a voltage source thus reduces by one the number of nonreference nodes at which we must apply KCL, regardless of whether the voltage source extends between two nonreference nodes or is connected between a node and the reference.

Now let us consider a circuit containing a dependent source. As our example, we select the op-amp connected as a voltage follower, Fig. 3-4*a*.

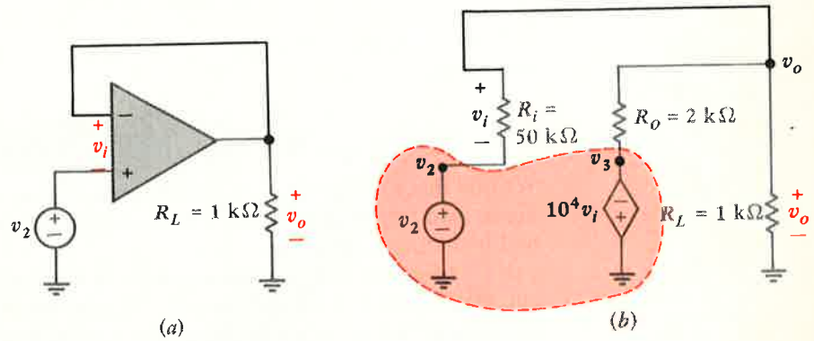


Fig. 3-4: (*a*) A voltage follower feeds a finite load R_L. (*b*) The op-amp is replaced with an equivalent circuit that includes a noninfinite R_i and a nonzero R_o. Three node-to-reference voltages are assigned, and one supernode is indicated.

This is the same circuit we investigated in the last section of Chapter 2, except that a finite load resistance $R_L = 1$ kΩ now appears between the output terminal and ground. We represent the op-amp by a model that includes a noninfinite input resistance, $R_i = 50$ kΩ, and a nonzero output resistance, $R_o = 2$ kΩ, as shown in the circuit of Fig. 3-4*b*; we assume a typical value of $A = 10^4$.

Ground is selected as the reference node, and the three nonreference nodes are assigned the voltages, v_2, v_o, and v_3. We note that the independent voltage source v_2 causes the v_2 node and the reference node to form a supernode; moreover, the dependent voltage source forces us to consider the v_3 node and the reference node as a supernode also. Thus, the v_2, v_o, and reference nodes form one large supernode, shown by the shaded, broken-line enclosure in Fig. 3-4*b*. Since the supernode includes the reference node, we will not write a KCL equation for it. The only KCL equation to be written is that at the v_o node. It is

$$\frac{v_o - v_2}{50\,000} + \frac{v_o - v_3}{2000} + \frac{v_o}{1000} = 0 \tag{6}$$

Let us set the independent source $v_2 = 1$ V. There are now two unknown node voltages, v_o and v_3 in (6), and no other (independent) KCL equations can be written. However, we must still express the voltage of each voltage source extending from node to node (and thus inside the broken-line enclosure) in terms of the node voltages, and we must also express the control of the dependent source (here, the voltage v_i) in terms of the node voltages.

First, we look at all the voltage sources inside the supernode. The source v_2 has been set equal to 1 V, and furthermore the node voltage itself was designated v_2. If we had been foolish enough to call it v_A, for example, then we should have to write the trivial equation, $v_A = v_2$. Next is the source Av_i. Since it is connected between node 3 and ground, we have

$$v_3 = -10^4 v_i$$

Finally, we must relate the currents or voltages on which the controlled sources depend to the node voltages. Here, v_i is defined across R_i, and

$$v_i = v_o - v_2 = v_o - 1$$

To solve (6) for v_o, we let $v_3 = -10^4(v_o - 1)$, obtaining one equation in one unknown,

$$\frac{v_o - 1}{50\,000} + \frac{v_o + 10^4(v_o - 1)}{2000} + \frac{v_o}{1000} = 0$$

We find that $v_o = 0.999\,700$ V, and thus the output voltage closely equals the input even for an op-amp that has relatively low gain, low input resistance, and high output resistance.

In passing, we note that the negative of the first term in (6) is the current supplied by the 1-V source, here $(1 - v_o)/50\,000 = 6.00$ nA, an exceedingly small value that is not apt to disturb the most delicate of sources. In contrast, the output current is the third term in (6), $v_o/1000 = 1.000$ mA, over 10^5 times as large. Thus the voltage follower can deliver much more current and power to the load than it draws from the source. In doing so it is not violating the conservation of energy, but merely drawing power from the dc supplies, which are usually not shown.

Let us summarize the method by which we may obtain a set of nodal equations for any resistive circuit:

1. Make a neat, simple, circuit diagram. Indicate all element and source values. Each source should have its reference symbol.
2. Assuming that the circuit has N nodes, choose one of these nodes as a reference node. Then write the node voltages $v_1, v_2, \ldots, v_{N-1}$ at their respective nodes, remembering that each node voltage is understood to be measured with respect to the chosen reference.
3. If the circuit contains only current sources, apply Kirchhoff's current law at each nonreference node. To obtain the conductance matrix if a circuit has only independent current sources, equate the total current leaving each node through all conductances to the total source current entering that node, and order the terms from v_1 to v_{N-1}. For each dependent current source present, relate the source current and the controlling quantity to the variables $v_1, v_2, \ldots, v_{N-1}$, if they are not already in that form.
4. If the circuit contains voltage sources, form a supernode about each one by enclosing the source and its two terminals within a broken-line enclosure, thus reducing the number of nodes by one for each voltage source that is present. The assigned node voltages should not be changed. Using these assigned node-to-reference voltages, apply KCL at each of the nodes or supernodes (that do not contain the reference node) in this modified circuit. Relate each source voltage to the variables v_1, v_2, $\ldots$, v_{N-1}, if it is not already in that form.

With these suggestions in mind, let us consider the circuit displayed in Fig. 3-5, one which contains all four types of sources and has five nodes. We

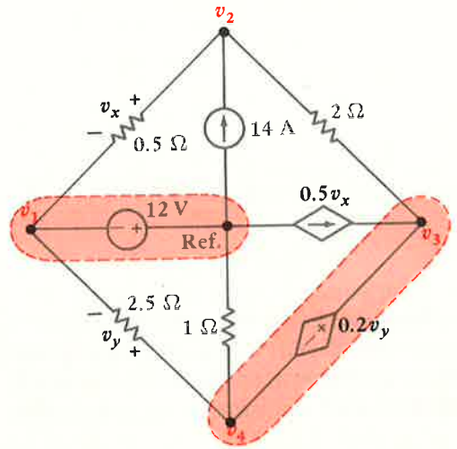


Fig. 3-5: A five-node circuit containing all of the four different types of sources.

select the central node as the reference, and assign v_1 to v_4 in a clockwise direction starting from the left node.

After establishing a supernode about each voltage source, we see that we need to write KCL equations only at node 2 and at the supernode containing both nodes 3 and 4 and the dependent voltage source. No extra equation need be written for the supernode which contains node 1 and the independent voltage source; it is obvious that $v_1 = -12$ V.

At node 2,

$$\frac{v_2 - v_1}{0.5} + \frac{v_2 - v_3}{2} = 14$$

while at the 3-4 supernode,

$$\frac{v_3 - v_2}{2} - 0.5v_x + \frac{v_4}{1} + \frac{v_4 - v_1}{2.5} = 0$$

We next relate the source voltages to the node voltages:

$$v_1 = -12$$

$$v_3 - v_4 = 0.2v_y = 0.2(v_4 - v_1)$$

And finally we express the dependent current source in terms of the assigned variables:

$$0.5v_x = 0.5(v_2 - v_1)$$

Thus, we obtain four equations in the four node voltages:

$$-2v_1 + 2.5v_2 - 0.5v_3 = 14$$

$$v_1 = -12$$

$$0.1v_1 - v_2 + 0.5v_3 + 1.4v_4 = 0$$

$$0.2v_1 + v_3 - 1.2v_4 = 0$$

to which the solutions are

$$v_1 = -12 \quad \text{V}$$

$$v_2 = -4 \quad \text{V}$$

$$v_3 = 0$$

$$v_4 = -2 \quad \text{V}$$

Drill Problems

3-1. Use nodal analysis to find v_y in the circuit shown in Fig. 3-6 if element A is: (a) a 2-A current source, arrow pointing right; (b) an 8-Ω resistor; (c) a 10-V voltage source, the positive reference on the right.

Ans: −20; −16; −6.91 V

3-2. Use nodal analysis to find v_y in the circuit of Fig. 3-6 if element A is: (a) a dependent current source, $0.2v_x$, arrow pointing left; (b) a dependent voltage source, $3i_Q$, the positive reference on the left; (c) an open circuit; (d) a short circuit.

Ans: 49.3; −14.14; −22.7; −8.73 V

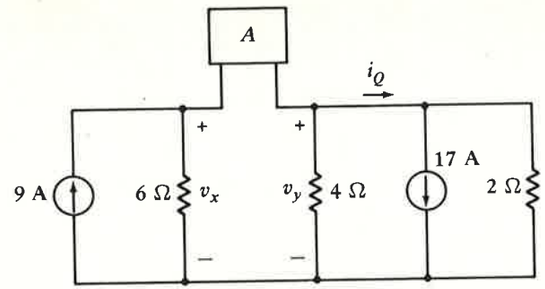


Fig. 3-6: See Drill Probs. 3-1 and 3-2.

3-3 Mesh Analysis

The technique of nodal analysis described in the preceding section is completely general and can always be applied to any electrical network. This is not the only method for which a similar claim can be made, however. In particular, we shall meet a generalized nodal analysis method and a technique known as *loop analysis* in the concluding sections of this chapter.

First, however, let us consider a method known as *mesh analysis*. Even though this technique is not applicable to every network, it can be applied to most of the networks we shall need to analyze, and it is probably used more often than it should be; other methods are often simpler. Mesh analysis is applicable only to those networks which are planar, a term we hasten to define.

If it is possible to draw the diagram of a circuit on a plane surface in such a way that no branch passes over or under any other branch, then that circuit is said to be a *planar* circuit. Thus, Fig. 3-7a shows a planar network, Fig. 3-7b shows a nonplanar network, and Fig. 3-7c shows a planar network, although it is drawn in such a way as to make it *appear* nonplanar at first glance.

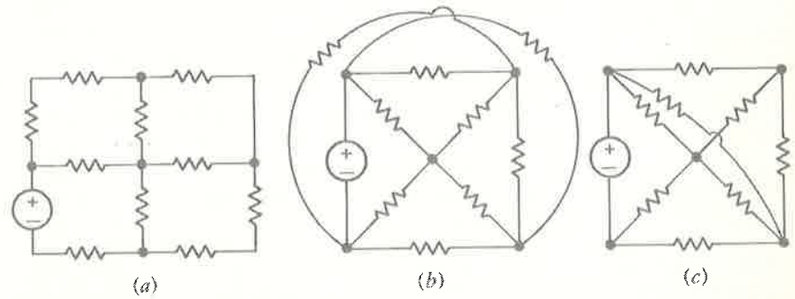


Fig. 3-7: (a) A planar network can be drawn on a plane surface without crossovers. (b) A nonplanar network cannot be drawn on a plane surface without at least one crossover. (c) A planar network can be drawn so that it may look nonplanar.

In the second chapter, the terms *path*, *closed path*, and *loop* were defined. Before we define a mesh, let us consider the sets of branches drawn with heavy lines in Fig. 3-8. The first set of branches is not a path since four branches are connected to the center node, and it is of course also not a loop. The second set of branches does not constitute a path since it is traversed

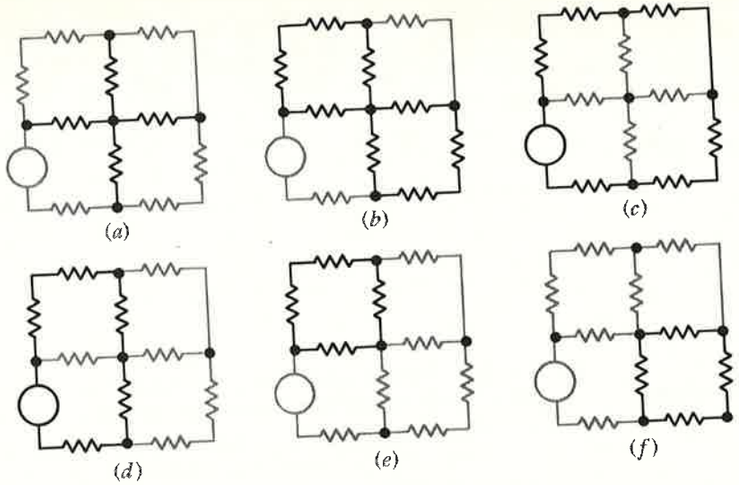


Fig. 3-8: (*a*) The set of branches identified by the heavy lines is neither a path nor a loop. (*b*) The set of branches here is not a path, since it can be traversed only by passing through the central node twice. (*c*) This path is a loop but not a mesh, since it encloses other loops. (*d*) This path is also a loop but not a mesh. (*e*) and (*f*) Each of these paths is both a loop and a mesh.

only by passing through the central node twice. The remaining four paths are all loops. The circuit contains 11 branches.

The mesh is a property of a planar circuit and is not defined for a nonplanar circuit. We define a *mesh* as a loop which does not contain any other loops within it. Thus, the loops indicated in Fig. 3-8*c* and *d* are not meshes, whereas those of *e* and *f* are meshes. Once a circuit has been drawn neatly in planar form, it often has the appearance of a multipaned window; each pane in the window may be considered to be a mesh.

If a network is planar, mesh analysis can be used to accomplish its analysis. This technique involves the concept of a *mesh current*, which we shall introduce by considering the analysis of the two-mesh circuit of Fig. 3-9.

As we did in the single-loop circuit, we shall begin by assuming a current through one of the branches. Let us call the current flowing to the right through the 6-Ω resistor i_1. We intend to apply Kirchhoff's voltage law around each of the two meshes, and the resulting two equations are sufficient to determine two unknown currents. Therefore we select a second current i_2 flowing to the right in the 4-Ω resistor. We might also choose to call the current flowing downward through the central branch i_3, but it is evident from Kirchhoff's current law that i_3 may be expressed in terms of the two previously assumed currents as $(i_1 - i_2)$. The assumed currents are shown in Fig. 3-9.

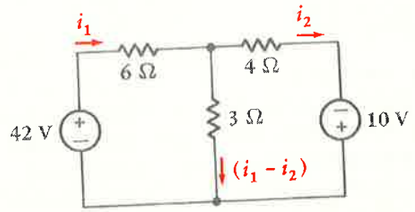


Fig. 3-9: Two currents, i_1 and i_2, are assumed in a two-mesh circuit.

Following the method of solution for the single-loop circuit, we now apply Kirchhoff's voltage law to the left-hand mesh,

$$-42 + 6i_1 + 3(i_1 - i_2) = 0$$

or

$$9i_1 - 3i_2 = 42 \tag{7}$$

and then to the right-hand mesh,

$$-3(i_1 - i_2) + 4i_2 - 10 = 0$$

or

$$-3i_1 + 7i_2 = 10 \tag{8}$$

Equations (7) and (8) are independent equations; one cannot be derived from the other.[3] There are two equations and two unknowns, and the solution is easily obtained: i_1 is 6 A, i_2 is 4 A, and $(i_1 - i_2)$ is therefore 2 A. The voltage and power relationships may be quickly obtained if desired.

If our circuit had contained M meshes, then we should have had to assume M branch currents and write M independent equations.[4] The solution in general may be systematically obtained through the use of determinants.

Now let us consider this same problem in a slightly different manner by using mesh currents. We define a *mesh current* as a current which flows only around the perimeter of a mesh. If we label the left-hand mesh of our problem as mesh 1, then we may establish a mesh current i_1 flowing in a clockwise direction about this mesh. A mesh current is indicated by a curved arrow that almost closes on itself and is drawn inside the appropriate mesh, as shown in Fig. 3-10. The mesh current i_2 is established in the remaining mesh, again in a clockwise direction. Although the directions are arbitrary, we shall always choose clockwise mesh currents because a certain error-minimizing symmetry then results in the equations.

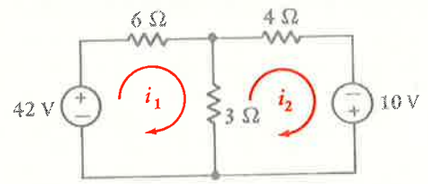


Fig. 3-10: A clockwise mesh current is assigned to each mesh of a planar circuit.

We no longer have a current or current arrow shown directly on each branch in the circuit. The current through any branch must be determined by considering the mesh currents flowing in every mesh in which that branch appears. This is not difficult because it is obvious that no branch can appear in more than two meshes. For example, the 3-Ω resistor appears in both meshes, and the current flowing downward through it is $(i_1 - i_2)$. The 6-Ω resistor appears only in mesh 1, and the current flowing to the right in that branch is equal to the mesh current i_1.

A mesh current may often be identified as a branch current, as i_1 and i_2 are

[3] It will be shown in Sec. 3-8 that mesh equations are always independent.
[4] The proof of this statement will be found in Sec. 3-8.

identified above. This is not always true, however, for consideration of a square nine-mesh network soon shows that the central mesh current cannot be identified as the current in any branch.

One of the greatest advantages in the use of mesh currents is the fact that Kirchhoff's current law is automatically satisfied. If a mesh current flows into a given node, it obviously flows out of it also.

We therefore may turn our attention to the application of KVL to each mesh. For the left-hand mesh,

$$-42 + 6i_1 + 3(i_1 - i_2) = 0$$

while for the right-hand mesh,

$$3(i_2 - i_1) + 4i_2 - 10 = 0$$

and these two equations are equivalent to (7) and (8).

Let us next consider the five-node, seven-branch, three-mesh circuit shown in Fig. 3-11. The three required mesh currents are assigned as indicated, and we methodically apply KVL about each mesh:

$$-7 + 1(i_1 - i_2) + 6 + 2(i_1 - i_3) = 0$$
$$1(i_2 - i_1) + 2i_2 + 3(i_2 - i_3) = 0$$
$$2(i_3 - i_1) - 6 + 3(i_3 - i_2) + 1i_3 = 0$$

Simplifying,

$$3i_1 - i_2 - 2i_3 = 1$$
$$-i_1 + 6i_2 - 3i_3 = 0$$
$$-2i_1 - 3i_2 + 6i_3 = 6$$

and Cramer's rule leads to the formulation for i_3:

$$i_3 = \frac{\begin{vmatrix} 3 & -1 & 1 \\ -1 & 6 & 0 \\ -2 & -3 & 6 \end{vmatrix}}{\begin{vmatrix} 3 & -1 & -2 \\ -1 & 6 & -3 \\ -2 & -3 & 6 \end{vmatrix}} = \frac{117}{39} = 3 \quad \text{A}$$

The other mesh currents are $i_1 = 3$ A, and $i_2 = 2$ A.

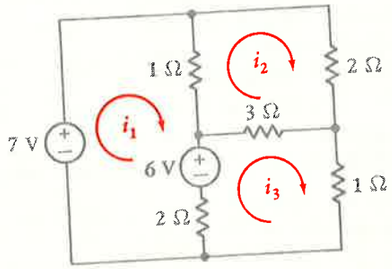


Fig. 3-11: Mesh currents i_1, i_2, and i_3 are assumed in a five-node, seven-branch, three-mesh circuit.

Again we notice that we have a denominator determinant that is symmetrical about the major diagonal and has positive terms on the major diagonal and zero or negative terms off it. This occurs for circuits that contain only independent voltage sources when clockwise mesh currents are assigned, where the elements appearing in the first row of the determinant are the ordered coefficients of $i_1, i_2, \ldots, i_M$ in the KVL equation about the first mesh, where the second row corresponds to the second mesh, and so on. This symmetrical array appearing in the denominator is the determinant of the *resistance matrix* of the network,

$$\mathbf{R} = \begin{bmatrix} 3 & -1 & -2 \\ -1 & 6 & -3 \\ -2 & -3 & 6 \end{bmatrix}$$

How must we modify this straightforward procedure when a current source is present in the network? Taking our lead from nodal analysis (and duality), we should feel that there are two possible methods. First, we could assign an unknown voltage across the current source, apply KVL around each mesh as before, and then relate the source current to the assigned mesh currents. This is generally the more difficult approach.

A better technique is one that is quite similar to the supernode approach in nodal analysis. There we formed a supernode, completely enclosing the voltage source inside the supernode and reducing the number of nonreference nodes by one for each voltage source. Now we create a kind of "supermesh" from two meshes that have a current source as a common element; the current source is in the interior of the supermesh. We thus reduce the number of meshes by one for each current source present. If the current source lies on the perimeter of the circuit, then the single mesh in which it is found is ignored.[5] Kirchhoff's voltage law is applied only to those meshes or supermeshes in the modified network.

As an example of this procedure, consider the network shown in Fig. 3-12, in which a 7-A independent current source is in the common boundary of two meshes. Mesh currents i_1, i_2, and i_3 are assigned, and the current source

[5] Such a current source is a common element with the mesh that "encloses" the outside of the entire circuit. Just as we do not write a nodal equation at the reference node, we do not write a KVL equation for this external mesh.

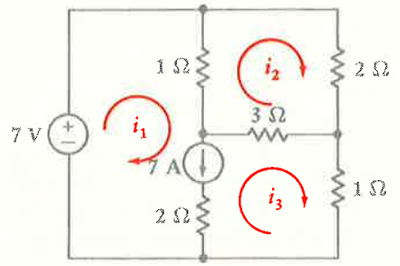


Fig. 3-12: Mesh analysis is applied to this circuit containing a current source by writing the KVL equation about the loop: 7 V, 1 Ω, 3 Ω, 1 Ω.

causes us to create a supermesh whose interior is that of meshes 1 and 3. Applying KVL about this loop,

$$-7 + 1(i_1 - i_2) + 3(i_3 - i_2) + 1i_3 = 0$$

or

$$i_1 - 4i_2 + 4i_3 = 7 \tag{9}$$

and around mesh 2,

$$1(i_2 - i_1) + 2i_2 + 3(i_2 - i_3) = 0$$

or

$$-i_1 + 6i_2 - 3i_3 = 0 \tag{10}$$

Finally, the source current is related to the assumed mesh currents,

$$i_1 - i_3 = 7 \tag{11}$$

Solving (9) through (11), we have

$$i_3 = \frac{\begin{vmatrix} -1 & 6 & 0 \\ 1 & -4 & 7 \\ 1 & 0 & 7 \end{vmatrix}}{\begin{vmatrix} -1 & 6 & -3 \\ 1 & -4 & 4 \\ 1 & 0 & -1 \end{vmatrix}} = \frac{28}{14} = 2 \quad \text{A}$$

We may also find that $i_1 = 9$ A and $i_2 = 2.5$ A.

The presence of one or more dependent sources merely requires each of these source quantities and the variable on which it depends to be expressed in terms of the assigned mesh currents. In Fig. 3-13, for example, we note that both a dependent and an independent current source are included in the network. Three mesh currents are assigned and KVL is applied to mesh 2:

$$1(i_2 - i_1) + 2i_2 + 3(i_2 - i_3) = 0$$

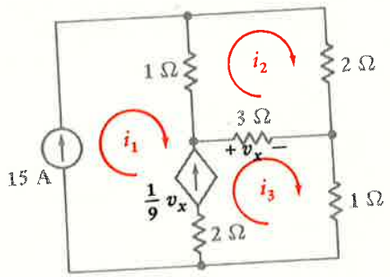


Fig. 3-13: The presence of two current sources in this three-mesh circuit makes it necessary to apply KVL only once, around mesh 2.

The current sources appear in meshes 1 and 3. Since the 15-A source is located on the perimeter of the circuit, we may eliminate mesh 1 from consideration. Then, the dependent current source is on the perimeter of the modified network, and thus we avoid any equation writing for mesh 3. Only mesh 2 remains, and we already have an equation for it. We therefore turn our attention to the source quantities, obtaining

$$i_1 = 15$$

and

$$\tfrac{1}{9} v_x = i_3 - i_1 = \tfrac{1}{9}[3(i_3 - i_2)]$$

Thus,

$$-i_1 + 6i_2 - 3i_3 = 0$$

$$i_1 = 15$$

$$-i_1 + \tfrac{1}{3}i_2 + \tfrac{2}{3}i_3 = 0$$

from which we have $i_1 = 15$, $i_2 = 11$, and $i_3 = 17$ A. We might note that we wasted a little time in assigning a mesh current i_1 to the left mesh; we should simply have indicated a mesh current and labeled it 15 A.

Let us summarize the method by which we may obtain a set of mesh equations for a resistive circuit:

1 Make certain that the network is a planar network. If it is nonplanar, mesh analysis is not applicable.
2 Make a neat, simple, circuit diagram. Indicate all element and source values. Resistance values are preferable to conductance values. Each source should have its reference symbol.
3 Assuming that the circuit has M meshes, assign a clockwise mesh current in each mesh, $i_1, i_2, \ldots, i_M$.
4 If the circuit contains only voltage sources, apply Kirchhoff's voltage law around each mesh. To obtain the resistance matrix if a circuit has only independent voltage sources, equate the clockwise sum of all the resistor voltages to the counterclockwise sum of all the source voltages, and order the terms, from i_1 to i_M. For each dependent voltage source present, relate the source voltage and the controlling quantity to the variables $i_1, i_2, \ldots, i_M$, if they are not already in that form.
5 If the circuit contains current sources, create a supermesh for each current source that is common to two meshes by applying KVL around the larger loop formed by the branches that are not common to the two meshes; KVL need not be applied to a mesh containing a current source that lies on the perimeter of the entire circuit. The assigned mesh currents should not be changed. Relate each source current to the variables $i_1, i_2, \ldots, i_M$, if it is not already in that form.

Drill Problems

3-3. Use mesh analysis to find v_A in the circuit of Fig. 3-14 if element A is: (*a*) a 4-V voltage source, the positive reference at the top; (*b*) a 9-Ω resistor; (*c*) a 600-mA current source, arrow directed downward.

Ans: 23.7; 23.6; 23.9 V

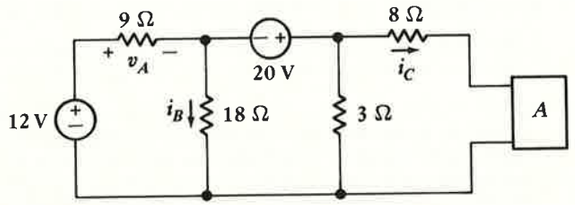


Fig. 3-14: See Drill Probs. 3-3 and 3-4.

3-4. Use mesh analysis to find i_C in Fig. 3-14 if element A is: (a) a dependent voltage source, $0.2v_A$, the positive reference at the top; (b) a dependent current source, $0.5i_B$, arrow directed downward. *Ans:* 0.462; −0.281 A

3-4 Linearity and superposition

All the circuits which we have analyzed up to now (and which we shall analyze later) are linear circuits. At this time we must be more specific in defining a linear circuit. Having done this, we can then consider the most important consequence of linearity, the principle of superposition. This principle is very basic and will appear repeatedly in our study of linear circuit analysis. As a matter of fact, the nonapplicability of superposition to nonlinear circuits is the reason they are so difficult to analyze.

The principle of superposition states that the response (a desired current or voltage) at any point in a linear circuit having more than one independent source can be obtained as the sum of the responses caused by each independent source acting alone. In the following discussion, we shall investigate the meaning of "linear" and "acting alone." We shall also take note of a slightly broader form of the theorem.

Let us first define a *linear element* as a passive element that has a linear voltage-current relationship. By a "linear voltage-current relationship" we shall mean simply that multiplication of the time-varying current through the element by a constant K results in the multiplication of the time-varying voltage across the element by the same constant K. At this time, only one passive element has been defined, the resistor, and its voltage-current relationship

$$v(t) = Ri(t)$$

is obviously linear. As a matter of fact, if $v(t)$ is plotted as a function of $i(t)$, the result is a straight *line*. We shall see in Chap. 4 that the defining voltage-current equations for inductance and capacitance are also linear relationships, as is the defining equation for mutual inductance presented in Chap. 15.

We must also define a *linear dependent source* as a dependent current or voltage source whose output current or voltage is proportional only to the first power of some current or voltage variable in the circuit or to the sum of such quantities. That is, a dependent voltage source, $v_s = 0.6i_1 - 14v_2$, is linear, but $v_s = 0.6i_1^2$ and $v_s = 0.6i_1v_2$ are not.

We may now define a *linear circuit* as a circuit composed entirely of independent sources, linear dependent sources, and linear elements. From this definition, it is possible to show[6] that "the response is proportional to

[6] The proof involves first showing that the use of nodal analysis on the linear circuit can produce only linear equations of the form:

$$a_1v_1 + a_2v_2 + \cdots + a_Nv_N = b$$

where the a_i are constants (combinations of resistance or conductance values, constants appearing in dependent source expressions, 0, or ±1), the v_i are the unknown node voltages (responses), and b is an independent source value or a sum of independent source values. Given a set of such equations, if we multiply all the b's by K, then it is evident that the solution of this new set of equations will be the node voltages Kv_1, Kv_2, . . . , Kv_N.

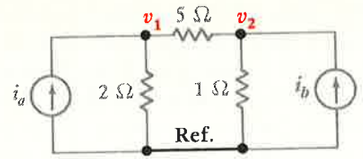


Fig. 3-15: A three-node circuit, containing two forcing functions, used to illustrate the superposition principle.

the source," or that multiplication of *all independent* source voltages and currents by a constant K increases all the current and voltage responses by the same factor K (including the dependent source voltage or current outputs).

The most important consequence of linearity is superposition. Let us develop the superposition principle by considering first the circuit of Fig. 3-15, which contains two independent sources, the current generators which force the currents i_a and i_b into the circuit. Sources are often called *forcing functions* for this reason, and the voltages which they produce between node 1 or 2 and the reference node may be termed *response functions*, or simply *responses*. Both the forcing functions and the responses may be functions of time.

The two nodal equations for this circuit are

$$0.7v_1 - 0.2v_2 = i_a \tag{12}$$

$$-0.2v_1 + 1.2v_2 = i_b \tag{13}$$

Now let us perform experiment x. We change the two forcing functions to i_{ax} and i_{bx}; the two unknown voltages will now be different, and we shall let them be v_{1x} and v_{2x}. Thus,

$$0.7v_{1x} - 0.2v_{2x} = i_{ax} \tag{14}$$

$$-0.2v_{1x} + 1.2v_{2x} = i_{bx} \tag{15}$$

We next perform experiment y by changing the source currents to i_{ay} and i_{by} and by letting the responses be v_{1y} and v_{2y},

$$0.7v_{1y} - 0.2v_{2y} = i_{ay} \tag{16}$$

$$-0.2v_{1y} + 1.2v_{2y} = i_{by} \tag{17}$$

These three sets of equations describe the same circuit with different source currents. Let us *add* or *superpose* the last two sets of equations. Adding (14) and (16),

$$(0.7v_{1x} + 0.7v_{1y}) - (0.2v_{2x} + 0.2v_{2y}) = i_{ax} + i_{ay} \tag{18}$$

$$0.7v_1 - 0.2v_2 = i_a \tag{12}$$

and adding (15) and (17),

$$-(0.2v_{1x} + 0.2v_{1y}) + (1.2v_{2x} + 1.2v_{2y}) = i_{bx} + i_{by} \tag{19}$$

$$-0.2v_1 + 1.2v_2 = i_b \tag{13}$$

where (12) has been written immediately below (18), and (13) below (19) for easy comparison.

The linearity of all these equations allows us to compare (18) with (12) and (19) with (13) and draw an interesting conclusion. If we select i_{ax} and i_{ay} such that their sum is i_a, select i_{bx} and i_{by} such that their sum is i_b, then the desired responses v_1 and v_2 may be found by *adding* v_{1x} to v_{1y} and v_{2x} to v_{2y}, respectively. In other words, we may perform experiment x and note the responses, perform experiment y and note the responses, and finally add the corresponding responses. These are the responses of the original circuit to independent sources which are the sums of the independent sources used in experiments x and y. This is the fundamental concept involved in the superposition principle.

It is evident that we may extend these results by breaking up either source current into as many pieces as we wish; there is no reason why we cannot perform experiments z and q also. It is only necessary that the algebraic sum of the pieces be equal to the original current.

The *superposition theorem* usually appears in a form similar to the following:

> In any linear resistive network containing several sources, the voltage across or the current through any resistor or source may be calculated by adding algebraically all the individual voltages or currents caused by each independent source acting alone, with all other independent voltage sources replaced by short circuits and all other independent current sources replaced by open circuits.

Thus if there are N independent sources, we perform N experiments. Each independent source is active in only one experiment, and only one independent source is active in each experiment. An inactive independent voltage source is identical with a short circuit, and an inactive independent current source is an open circuit. Note that *dependent* sources are in general active in *every* experiment.

The circuit used as an example above, however, should indicate that a much stronger theorem might be written; a group of independent sources may be made active and inactive collectively, if we wish. For example, suppose there are three independent sources. The theorem above states that we may find a given response by considering each of the three sources acting alone and adding the three results. Alternatively, we may find the response due to the first and second sources operating with the third inactive, and then add to this the response caused by the third source acting alone. This amounts to treating several sources collectively as a sort of supersource.

There is also no reason that an independent source must assume only its given value or a zero value in the several experiments; it is only necessary for the sum of the several values to be equal to the original value. An inactive source almost always leads to the simplest circuit, however.

Let us illustrate the application of the superposition principle by considering an example in which both types of independent source are present. For the circuit of Fig. 3-16, let us use superposition to write an expression for the

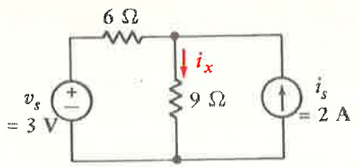


Fig. 3-16: A circuit, containing both an independent current and voltage source, which is easily analyzed by the superposition principle.

unknown branch current i_x. We may first set the current source equal to zero and obtain the portion of i_x due to the voltage source as 0.2 A. Then if we let the voltage source be zero and apply current division, the remaining portion of i_x is seen to be 0.8 A. We might write the answer in detail as

$$i_x = i_x|_{i_s=0} + i_x|_{v_s=0} = \frac{3}{6+9} + 2\frac{6}{6+9} = 0.2 + 0.8 = 1.0 \quad \text{A}$$

As an example of the application of the superposition principle to a circuit containing a dependent source, consider Fig. 3-17. We seek i_x, and we first open-circuit the 3-A source. The single mesh equation is

$$-10 + 2i'_x + 1i'_x + 2i'_x = 0$$

so that

$$i'_x = 2$$

Next, we short-circuit the 10-V source and write the single-node equation,

$$\frac{v''}{2} + \frac{v'' - 2i''_x}{1} = 3$$

and relate the dependent-source-controlling quantity to v'',

$$v'' = -2i''_x$$

We find

$$i''_x = -0.6$$

and, thus,

$$i_x = i'_x + i''_x = 2 - 0.6 = 1.4$$

It usually turns out that little if any time is saved in analyzing a circuit containing one or more dependent sources by use of the superposition principle, for there must always be at least two sources in operation: one independent source and all the dependent sources.

We must constantly be aware of the limitations of superposition. It is

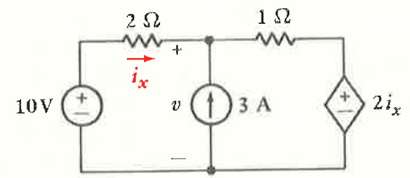


Fig. 3-17: Superposition may be used to analyze this circuit by first replacing the 3-A source by an open circuit and then replacing the 10-V source by a short circuit. The dependent voltage source is always active (unless $i_x = 0$).

applicable only to linear responses, and thus the most common nonlinear response—power—is not subject to superposition. For example, consider two 1-V batteries in series with a 1-Ω resistor. The power delivered to the resistor is obviously 4 W, but if we mistakenly try to apply superposition we might say that each battery alone furnished 1 W and thus the total power is 2 W. This is incorrect.

Drill Problem

3-5. Use superposition to find i_x in each of the circuits shown in Fig. 3-18. *Ans:* −175; 200; 50 mA

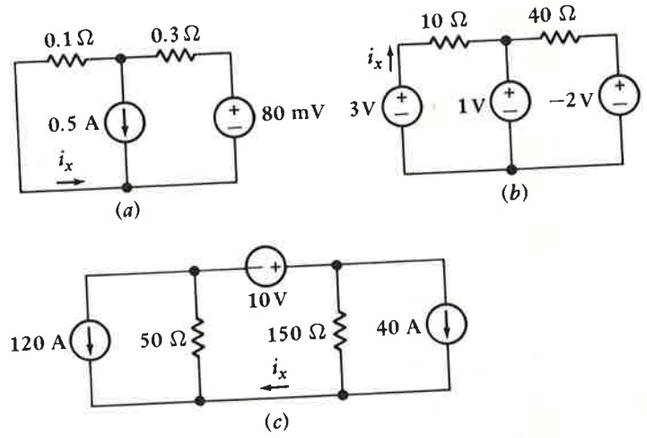


Fig. 3-18: See Drill Prob. 3-5.

3-5 Source transformations

In all our previous work we have been making continual use of *ideal* voltage and current sources; it is now time to take a step closer to reality by considering *practical* sources. These sources will enable us to make more realistic representations of physical devices. Having defined the practical sources, we shall then study methods whereby practical current and voltage sources may be interchanged without affecting the remainder of the circuit. Such sources will be called *equivalent* sources. Our methods will be applicable for both independent and dependent sources, although we shall see later that they are not as useful for dependent sources.

The ideal voltage source was defined as a device whose terminal voltage is independent of the current through it. A 1-V dc source produces a current of 1 A through a 1-Ω resistor and a current of 1 000 000 A through a 1-μΩ resistor; it may provide an unlimited amount of power. No such device exists practically, of course, and we agreed that a real physical voltage source might be represented by an ideal voltage source only as long as relatively small currents, or powers, were drawn from it. For example, an automobile storage battery may be approximated by an ideal dc voltage source if its current is limited to a few amperes. However, anyone who has ever tried to start an automobile with the headlights on must have observed that the lights dimmed perceptibly when the battery was asked to deliver the

heavy starter current, 100 A or more, in addition to the headlight current. Under these conditions, an ideal voltage source may be a very poor representation of the storage battery.

The ideal voltage source must be modified to account for the lowering of its terminal voltage when large currents are drawn from it. Let us suppose that we observe experimentally that a storage battery has a terminal voltage of 12 V when no current is flowing through it and a reduced voltage of 11 V when 100 A is flowing. Thus, a more accurate model might be an ideal voltage source of 12 V in series with a resistor across which 1 V appears when 100 A flows through it. The resistor must be 0.01 Ω, and the ideal voltage source and this series resistor comprise a *practical voltage source*. Thus, we are using the series combination of two ideal circuit elements, an independent voltage source and a resistor, to model a real device.

We should not expect to find such an arrangement of ideal elements inside our storage battery, of course. Any real device is characterized by a certain current-voltage relationship at its terminals, and our problem is to develop some combination of ideal elements that can furnish a similar current-voltage characteristic, at least over some useful range of current, voltage, or power.

This particular practical voltage source is shown connected to a general load resistor R_L in Fig. 3-19*a*. The terminal voltage of the practical source is the same as the voltage across R_L and is marked v_L.

Figure 3-19*b* shows a plot of load current i_L vs. load voltage v_L for this practical source. The KVL equation for the circuit of Fig. 3-19*a* may be written in terms of i_L and v_L:

$$12 = 0.01i_L + v_L$$

and thus

$$i_L = 1200 - 100v_L$$

This is a linear equation in i_L and v_L, and the plot in Fig. 3-19*b* is a straight line. Each point on the line corresponds to a different value of R_L. For example, the midpoint of the straight line is obtained when the load resistance is equal to the internal resistance of the practical source, $R_L = 0.01\ \Omega$. Here, the load voltage is only one-half the ideal source voltage.

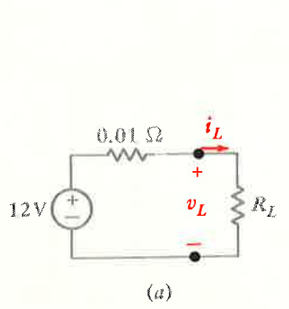


Fig. 3-19: (*a*) A practical source, which approximates the behavior of a certain 12-V storage battery, is shown connected to a load resistor R_L. (*b*) The relationship between i_L and v_L is linear.

When $R_L = \infty$ and no current whatsoever is being drawn by the load, the practical source is open-circuited and the terminal voltage, or open-circuit voltage, is $v_{Loc} = 12$ V. If, on the other hand, $R_L = 0$, thereby short-circuiting the load terminals, then a load current or short-circuit current, $i_{Lsc} = 1200$ A, would flow. In practice, such an experiment would probably result in the destruction of the short circuit, the battery, and any measuring instruments incorporated in the circuit.

Since the plot of i_L vs. v_L is a straight line for this practical voltage source, we should note that the values of v_{Loc} and i_{Lsc} uniquely determine the entire i_L-v_L curve.

The vertical broken line shows the i_L-v_L plot for an ideal voltage source; the terminal voltage remains constant for any value of load current. For the practical voltage source, the terminal voltage has a value near that of the ideal source only when the load current is relatively small.

Let us now consider a general practical voltage source, as shown in Fig. 3-20*a*. The voltage of the ideal source is v_s, and a resistance R_{sv}, called an *internal resistance* or *output resistance*, is placed in series with it. Again, we must note that the resistor is not one that is really present, or that we would wire or solder into the circuit, but merely serves to account for a terminal voltage which decreases as the load current increases. Its presence enables us to model the behavior of a physical voltage source more closely.

The linear relationship between v_L and i_L is

$$v_L = v_s - R_{sv} i_L \tag{20}$$

and this is plotted in Fig. 3-20*b*. The open-circuit voltage and short-circuit current are

$$v_{Loc} = v_s \tag{21}$$

$$i_{Lsc} = \frac{v_s}{R_{sv}} \tag{22}$$

Once again, these values are the intercepts for the straight line on Fig. 3-20*b*, and they serve to define it completely.

An ideal current source is also nonexistent in the real world; there is no physical device which will deliver a constant current, regardless of the load

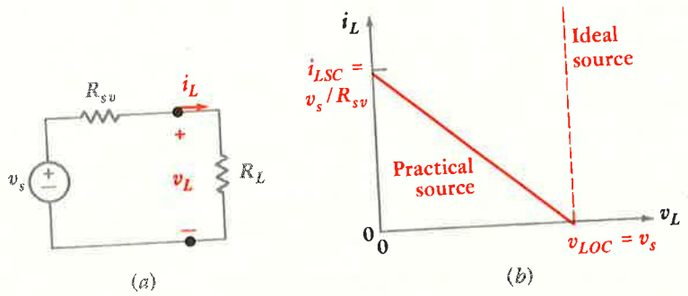


Fig. 3-20: (a) A general practical voltage source connected to a load resistor R_L. (*b*) The terminal voltage decreases as i_L increases and $R_L = v_L/i_L$ decreases.

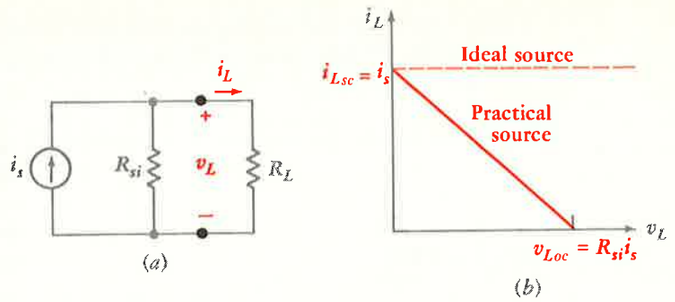


Fig. 3-21: (*a*) A general practical current source connected to a load resistor R_L. (*b*) The load current provided by the practical current source is shown as a function of the load voltage.

resistance to which it is connected or the voltage across its terminals. Certain transistor circuits will deliver a constant current to a wide range of load resistances, but the load resistance can always be made sufficiently large that the current through it becomes very small. Infinite power is simply never available.

A practical current source is defined as an ideal current source in parallel with an internal resistance R_{si}. Such a source is shown in Fig. 3-21*a*, and the current i_L and voltage v_L associated with a load resistance R_L are indicated. It is apparent that

$$i_L = i_s - \frac{v_L}{R_{si}} \tag{23}$$

which is again a linear relationship. The open-circuit voltage and the short-circuit current are:

$$v_{Loc} = R_{si} i_s \tag{24}$$

$$i_{Lsc} = i_s \tag{25}$$

The variation of load current with changing load voltage may be investigated by changing the value of R_L as shown in Fig. 3-21*b*. The straight line is traversed from the short-circuit or northwest end to the open-circuit termination at the southeast by increasing R_L from zero to infinite ohms. The midpoint occurs for $R_L = R_{si}$. It is evident that the load current i_L and the ideal source current i_s are approximately equal only for small values of load voltage, obtained with values of R_L that are small compared with R_{si}.

Having defined both practical sources, we are now ready to discuss their equivalence. We shall define two sources as being *equivalent* if they produce identical values of v_L and i_L when they are connected to identical values of R_L, no matter what the value of R_L may be. Since $R_L = 0$ and $R_L = \infty$ are two such values, then equivalent sources provide the same open-circuit voltage and short-circuit current. In other words, if we are given two equivalent sources, one a practical voltage source and the other a practical current source, each enclosed in a black box with only a single pair of terminals on it, then there is no way in which we can differentiate between the boxes by measuring current or voltage in a resistive load.

The conditions for equivalence are now quickly established. Since the open-circuit voltages must be equal, from Eqs. (21) and (24) we have

$$v_{Loc} = v_s = R_{si} i_s \tag{26}$$

The short-circuit currents are also equal, and Eqs. (22) and (25) lead to

$$i_{Lsc} = \frac{v_s}{R_{sv}} = i_s$$

It follows that

$$R_{sv} = R_{si} = R_s \tag{27}$$

and

$$v_s = R_s i_s \tag{28}$$

where we now let R_s represent the internal resistance of either practical source.

As an example of the use of these ideas, consider the practical current source shown in Fig. 3-22*a*. Since its internal resistance is 2 Ω, the internal resistance of the equivalent practical voltage source is also 2 Ω; the voltage of the ideal voltage source contained within the practical voltage source is (2)(3) = 6 V. The equivalent practical voltage source is shown in Fig. 3-22*b*.

To check the equivalence, let us visualize a 4-Ω resistor connected to each source. In both cases a current of 1 A, a voltage of 4 V, and a power of 4 W are associated with the 4-Ω load. However, we should note very carefully that the ideal current source is delivering a total power of 12 W, while the ideal voltage source is delivering only 6 W. Furthermore, the internal resistance of the practical current source is absorbing 8 W, whereas the internal resistance of the practical voltage source is absorbing only 2 W. Thus we see that the two practical sources are only equivalent with respect to what transpires at the load terminals; they are *not* equivalent internally!

A very useful power theorem may be developed with reference to a practical voltage or current source. For the practical voltage source (Fig. 3-20*a* with $R_{sv} = R_s$), the power delivered to the load R_L is

$$p_L = i_L^2 R_L = \frac{v_s^2 R_L}{(R_s + R_L)^2}$$

To find the value of R_L that absorbs a maximum power from the given practical source, we differentiate with respect to R_L:

$$\frac{dp_L}{dR_L} = \frac{(R_s + R_L)^2 v_s^2 - v_s^2 R_L (2)(R_s + R_L)}{(R_s + R_L)^4}$$

and equate the derivative to zero, obtaining,

$$2R_L(R_s + R_L) = (R_s + R_L)^2$$

or

$$R_s = R_L$$

Since the values, $R_L = 0$ and $R_L = \infty$, both give a minimum ($p_L = 0$), and since we have already developed the equivalence between practical voltage

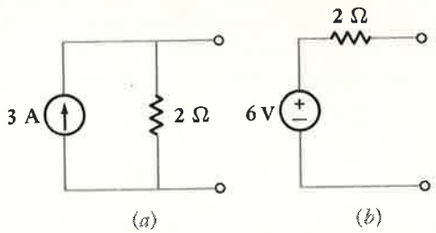


Fig. 3-22: (*a*) A given practical current source. (*b*) The equivalent practical voltage source: $R_{sv} = R_{si} = R_s$; $v_s = R_s i_s$.

and current sources, we have therefore proved the following *maximum power transfer* theorem:

> An independent voltage source in series with a resistance R_s or an independent current source in parallel with a resistance R_s delivers a maximum power to that load resistance R_L for which $R_L = R_s$.

Thus, the maximum power transfer theorem tells us that a 2-Ω resistor draws the greatest power (4.5 W) from either practical source of Fig. 3-22, whereas a resistance of 0.01 Ω receives the maximum power (3.6 kW) in Fig. 3-19.

Drill Problems

3-6. (*a*) Let $R_L = 80$ Ω in Fig. 3-23*a* and find i_L. (*b*) Transform the practical current source into a practical voltage source and again find i_L if $R_L = 80$ Ω. (*c*) Find the power supplied by the ideal source in each case. (*d*) What value of R_L will absorb a maximum power, and what is the value of that power?

Ans: 20 mA; 20 mA; 160 mW, 40 mW; 20 Ω, 50 mW

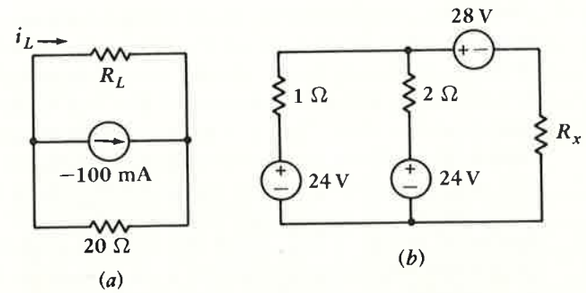


Fig. 3-23: See Drill Probs. 3-6 and 3-7.

3-7. Transform both 24-V practical sources in Fig. 3-23*b* into practical current sources, combine resistors and ideal current sources, then transform the resultant practical current source back into a practical voltage source, and combine ideal voltage sources. (*a*) If $R_x = 2$ Ω, find the power delivered to R_x. (*b*) What is the maximum power that can be delivered to any R_x? (*c*) What two values of R_x will have exactly 5 W delivered to them?

Ans: 4.5 W; 6 W; 0.280 and 1.587 Ω

3-6 Thévenin's and Norton's theorems

Now that we have the superposition principle, it is possible to develop two more theorems which will greatly simplify the analysis of many linear circuits. The first of these theorems is named after M. L. Thévenin, a French engineer working in telegraphy, who first published a statement of the theorem in 1883; the second may be considered a corollary of the first and is credited to E. L. Norton, a scientist formerly with the Bell Telephone Laboratories.

Let us suppose that we need to make only a partial analysis of a circuit; perhaps we wish to determine the current, voltage, and power delivered to a single load resistor by the remainder of the circuit, which may consist of any number of sources and resistors; or perhaps we wish to find the response for different values of the load resistance. Thévenin's theorem then tells us that it is possible to replace everything except the load resistor by an equivalent circuit containing only an independent voltage source in series with a resistor; the response measured at the load resistor will be unchanged. Using Norton's theorem, we obtain an equivalent composed of an independent current source in parallel with a resistor.

It should thus be apparent that one of the main uses of Thévenin's and Norton's theorems is the replacement of a large part of a network, often a complicated and uninteresting part, by a very simple equivalent. The new, simpler circuit enables us to make rapid calculations of the voltage, current, and power which the original circuit is able to deliver to a load. It also helps us to choose the best value of this load resistance. In a transistor power amplifier, for example, the Thévenin or Norton equivalent enables us to determine the maximum power that can be taken from the amplifier and the type of load that is required to accomplish a maximum transfer of power or to obtain maximum practical voltage or current amplification.

As an introductory example, consider the circuit shown in Fig. 3-24. The shaded regions separate the circuit into networks A and B; we shall assume that our main interest is in network B, which consists only of the load resistor R_L. Network A may be simplified by making repeated source transformations. We first treat the 12-V source and the 3-Ω resistor as a practical voltage source and replace it with a practical current source consisting of a 4-A source in parallel with 3 Ω. The parallel resistances are then combined into 2 Ω, and the practical current source which results is transformed back into a practical voltage source. The steps are indicated in Fig. 3-25, the final result appearing in Fig. 3-25d. From the viewpoint of the load resistor R_L, this circuit (the Thévenin equivalent) is equivalent to the original circuit; from our viewpoint, the circuit is much simpler and we can now easily compute the power delivered to the load. It is

$$p_L = \left(\frac{8}{9 + R_L}\right)^2 R_L$$

Furthermore we can see from the equivalent circuit that the maximum voltage which can be obtained across R_L is 8 V when $R_L = \infty$; a quick transformation of network A to a practical current source (the Norton equivalent) indicates that the maximum current which may be delivered to the load is $\frac{8}{9}$ A

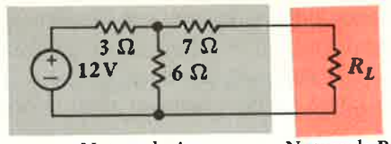


Fig. 3-24: A simple resistive circuit is divided into network A, in which we have no detailed interest, and network B, a load resistor with which we are fascinated.

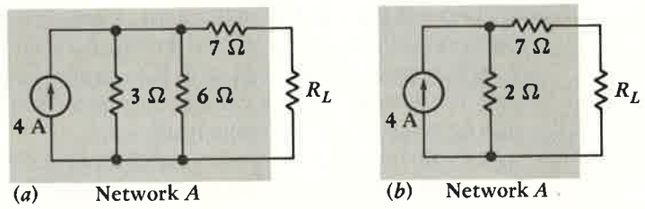


Fig. 3-25: The source transformations and resistance combinations involved in simplifying network A are shown in order. The result, given in (d), is the Thévenin equivalent.

for $R_L = 0$; and the maximum power transfer theorem shows that a maximum power is delivered to R_L when R_L is 9 Ω. None of these facts is readily apparent from the original circuit.

If network A had been more complicated, the number of source transformations and resistance combinations necessary to obtain the Thévenin or Norton equivalent could easily become prohibitive; also, with dependent sources present, the method of source transformation is usually inapplicable. Thévenin's and Norton's theorems allow us to find the equivalent circuit much more quickly and easily, even in more complicated circuits.

Let us now state *Thévenin's theorem* formally:

> Given any linear circuit, rearrange it in the form of two networks A and B that are connected together by two resistanceless conductors. If either network contains a dependent source, its control variable must be in that same network. Define a voltage v_{oc} as the open-circuit voltage which would appear across the terminals of A if B were disconnected so that no current is drawn from A. Then all the currents and voltages in B will remain unchanged if A is killed (all independent voltage sources and independent current sources in A replaced by short circuits and open circuits, respectively) and an independent voltage source v_{oc} is connected, with proper polarity, in series with the dead (inactive) A network.

The terms *killed* and *dead* are a little bloodthirsty, but they are descriptive and concise, and we shall use them in a friendly way. Moreover, it is possible that network A may only be sleeping, for it may still contain *dependent* sources which come to life whenever their controlling currents or voltages are nonzero.

Let us see if we can apply Thévenin's theorem successfully to the circuit we considered in Fig. 3-24. Disconnecting R_L, voltage division enables us to determine that v_{oc} is 8 V. Killing the A network, that is, replacing the 12-V source by a short circuit, we see looking back into the dead A network a 7-Ω resistor connected in series with the parallel combination of 6 Ω and 3 Ω. Thus the dead A network can be represented here by simply a 9-Ω resistor. This agrees with the previous result.

The equivalent circuit we have obtained is completely independent of the B network, because we have been instructed first to remove the B network and measure the open-circuit voltage produced by the A network, an operation which certainly does not depend on the B network in any way, and then to place the inactive A network in series with a voltage source v_{oc}. The B network is mentioned in the theorem and proof only to indicate that an equivalent for A may be obtained *no matter what arrangement of elements is connected to the A network;* the B network represents this general network.

A proof of Thévenin's theorem in the form in which we have stated it is rather lengthy, and therefore it has been placed in Appendix 3 where the curious or rigorous may peruse it.

There are several points about the theorem which deserve emphasis. First, the only restriction that we must impose on A or B, other than requiring that the original circuit composed of A and B be a linear circuit, is that all the dependent sources in A have their control variables in A, and similarly for B. No restrictions were imposed on the complexity of A or B; either one may contain any combination of independent voltage or current sources, linear dependent voltage or current sources, resistors, or any other circuit elements which are linear. The general nature of the theorem (and its proof) will enable it to be applied to networks containing inductors and capacitors, which are linear passive circuit elements to be defined in the following chapter. At this time, however, resistors are the only passive circuit elements which have been defined, and the application of Thévenin's theorem to resistive networks is a particularly simple special case. The dead A network can be represented by a single equivalent resistance, R_{th}. If A is an active *resistive* network, then it is obvious that the inactive A network may be replaced by a single equivalent resistance, which we shall also call the Thévenin resistance, since it is once again the resistance viewed at the terminals of the inactive A network.

Norton's theorem bears a close resemblance to Thévenin's theorem, another consequence of duality. As a matter of fact, the two statements will be used as an example of dual language when the duality principle is discussed in the following chapter.

Norton's theorem may be stated as follows:

> Given any linear circuit, rearrange it in the form of two networks A and B that are connected together by two resistanceless conductors. If either network contains a dependent source, its control variable must be in that same network. Define a current i_{sc} as the short-circuit current which would appear at the terminals of A if B were short-circuited so that no voltage is provided by A. Then all the voltages and currents in B will remain unchanged if A is killed (all independent current sources and independent voltage sources in A replaced by open circuits and short circuits, respectively) and an independent current source i_{sc} is connected, with proper polarity, in parallel with the dead (inactive) A network.

The Norton equivalent of an active resistive network is the Norton current source i_{sc} in parallel with the Thévenin resistance R_{th}.

There is an important relationship between the Thévenin and Norton equivalents of an active *resistive* network. The relationship may be obtained by applying a source transformation to either equivalent network. For example, if we transform the Norton equivalent, we obtain a voltage source $R_{th}i_{sc}$ in series with the resistance R_{th}; this network is in the form of the Thévenin equivalent, and thus

$$v_{oc} = R_{th}i_{sc} \tag{29}$$

In resistive circuits containing *dependent* sources as well as independent sources, we shall often find it more convenient to determine either the Thévenin or Norton equivalent by finding both the open-circuit voltage and the short-circuit current and then determining the value of R_{th} as their quotient. It is therefore advisable to become adept at finding both open-circuit voltages and short-circuit currents, even in the simple problems which follow. If the Thévenin and Norton equivalents are determined independently, (29) may serve as a useful check.

Let us consider four examples of the determination of a Thévenin or Norton equivalent circuit. The first is shown in Fig. 3-26*a*; the Thévenin and Norton equivalents are desired for the network faced by the 1-kΩ resistor. That is, network B is this resistor, and network A is the remainder of the given circuit.

This circuit contains no dependent sources, and the easiest way to find the Thévenin equivalent is to determine R_{th} for the dead network directly, followed by a calculation of either v_{oc} or i_{sc}. We first kill both independent sources to determine the form of the dead A network. With the 4-V source short-circuited and the 2-mA source open-circuited, the result is the series combination of a 2-kΩ and 3-kΩ resistor, or the equivalent, a 5-kΩ resistor. The open-circuit voltage is easily determined by superposition. With only the 4-V source operating, the open-circuit voltage is 4 V; when only the 2-mA source is on, the open-circuit voltage is also 4 V; with both independent

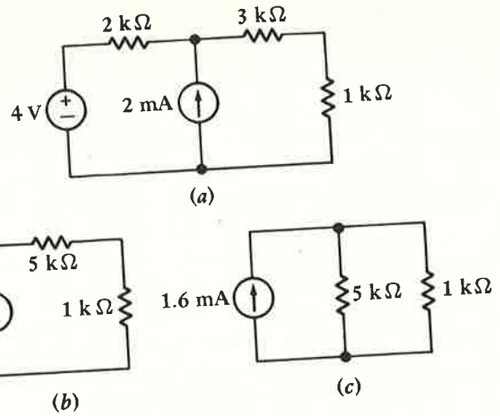


Fig. 3-26: (*a*) A given circuit in which the 1-kΩ resistor is identified as network *B*. (*b*) The Thévenin equivalent is shown for network *A*. (*c*) The Norton equivalent is shown for network *A*.

sources operating, we see that $v_{oc} = 4 + 4 = 8$ V. This determines the Thévenin equivalent, shown in Fig. 3-26*b*, and from it the Norton equivalent of Fig. 3-26*c* can be drawn quickly. As a check, let us determine i_{sc} for the given circuit. We use superposition and a little current division:

$$i_{sc} = i_{sc}|_{4V} + i_{sc}|_{2mA} = \frac{4}{2+3} + 2\frac{2}{2+3} = 0.8 + 0.8 = 1.6 \quad \text{mA}$$

which completes the check.

As the second example, we consider the network *A* shown in Fig. 3-27, which contains both independent and dependent sources. The presence of the dependent source prevents us from determining R_{th} directly for the inactive network through resistance combination; instead, we find both v_{oc} and i_{sc}. To find v_{oc} we note that $v_x = v_{oc}$, and that the dependent source current

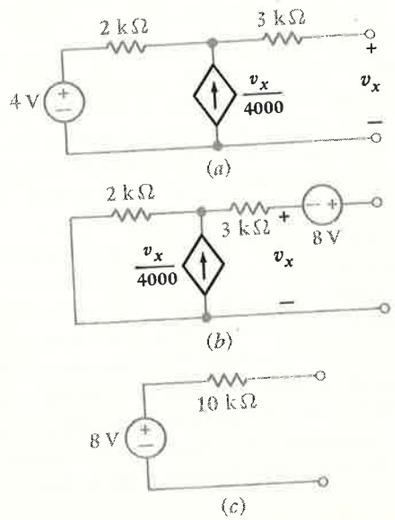


Fig. 3-27: (*a*) A given network whose Thévenin equivalent is desired. (*b*) A possible, but rather useless, form of the Thévenin equivalent. (*c*) The best form of the Thévenin equivalent for this linear resistive network.

must pass through the 2-kΩ resistor since there is an open circuit to the right. Summing voltages around the outer loop:

$$-4 + 2 \times 10^3 \left(\frac{-v_x}{4000}\right) + 3 \times 10^3(0) + v_x = 0$$

and

$$v_x = 8 = v_{oc}$$

By Thévenin's theorem, then, the equivalent could be formed with the dead *A* network in series with an 8-V source, as shown in Fig. 3-27*b*. This is correct, but is not very simple and not very helpful; in the case of linear resistive networks, we should certainly show a much simpler equivalent for the inactive *A* network, namely R_{th}. We therefore seek i_{sc}. Upon short-circuiting the output terminals in Fig. 3-27*a*, it is apparent that $v_x = 0$ and the dependent current source is zero. Hence, $i_{sc} = 4/(5 \times 10^3) = 0.8$ mA. Thus, $R_{th} = v_{oc}/i_{sc} = 8/(0.8 \times 10^{-3}) = 10$ kΩ, and the accepted Thévenin equivalent of Fig. 3-27*c* is obtained.

Another example for which we should find both v_{oc} and i_{sc} appears in Fig. 3-28. The circuit happens to be an op-amp connected as a voltage follower

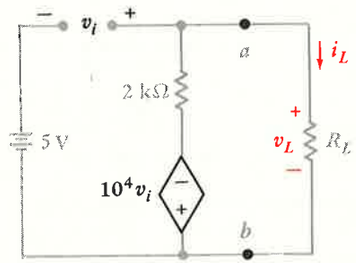


Fig. 3-28: The Thévenin equivalent of this voltage follower is desired for terminals *a*-*b*.

with $v_s = 5$ V, $R_i = \infty$, $A = 10^4$, and $R_o = 2$ kΩ. To find v_{Loc} we set $R_L = \infty$, or we simply consider it to be removed from the circuit. There now can be no current through the 2-kΩ resistor, and therefore

$$v_{Loc} = -10^4 v_i$$

where

$$v_i = v_{Loc} - 5$$

Therefore

$$v_{Loc} = \frac{10^4(5)}{10\,001} = 5.00 \quad \text{V}$$

Next we need a value for i_{Lsc}; so we replace R_L by a short circuit. Around the right mesh, KVL gives

$$10^4 v_i + 2000 i_{Lsc} = 0$$

while the application of KVL around the perimeter of the circuit gives

$$-5 - v_i = 0$$

Therefore

$$10^4(-5) + 2000 i_{Lsc} = 0$$

and

$$i_{Lsc} = 25.0 \quad \text{A}$$

We find R_{th} by the quotient,

$$R_{th} = \frac{v_{Loc}}{i_{Lsc}} = \frac{5.00}{25.0} = 0.200 \quad \Omega$$

Thus, the Thévenin equivalent presented to R_L at a-b by the voltage follower is 5.00 V in series with a very low value of resistance, 0.200 Ω.

As our final example, let us consider a network having a dependent source but no independent source, such as that shown in Fig. 3-29*a*. The network therefore qualifies already as the dead A network, and $v_{oc} = 0$. We thus seek the value of R_{th} represented by this two-terminal network. However, we cannot find v_{oc} and i_{sc} and take their quotient, for there is no independent source in the network and both v_{oc} and i_{sc} are zero. Let us, therefore, be a little tricky. We apply a 1-A source *externally*, measure the resultant voltage, and then set $R_{th} = v/1$. Referring to Fig. 3-29*b*, we see that $i = -1$ and

$$\frac{v - 1.5(-1)}{3} + \frac{v}{2} = 1$$

so that

$$v = 0.6 \quad \text{V}$$

and

$$R_{th} = 0.6 \quad \Omega$$

The Thévenin equivalent is shown in Fig. 3-29*c*.

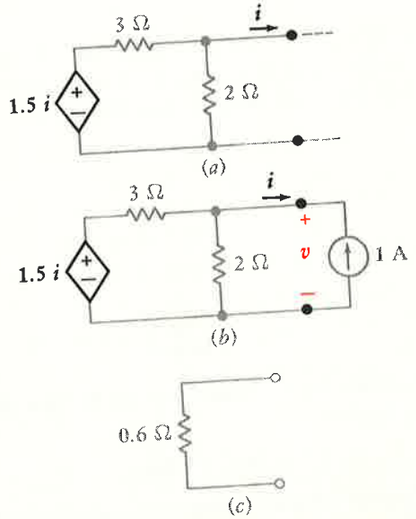


Fig. 3-29: (*a*) A network, containing no independent sources, whose Thévenin equivalent is desired. (*b*) R_{th} is numerically equal to v. (*c*) The Thévenin equivalent of (*a*).

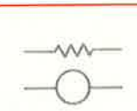
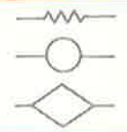
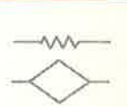
We have now looked at four examples in which we determined a Thévenin or Norton equivalent circuit. The first example (Fig. 3-26) contained only independent sources and resistors, and we were able to use several different methods on it. One involved calculating R_{th} for the dead network and then v_{oc} for the live network. We could also have found R_{th} and i_{sc}, or v_{oc} and i_{sc}.

In the second and third examples (Figs. 3-27 and 3-28), both independent and dependent sources were present, and the only method we used required us to find v_{oc} and i_{sc}. We could not easily find R_{th} for the dead network because the dependent source could not be made inactive.

The last example did not contain any independent sources, and we found R_{th} by applying 1 A and finding $v = 1 \times R_{th}$. We could also apply 1 V and determine $i = 1/R_{th}$. These Thévenin and Norton equivalents do not contain an independent source.

These important techniques and the types of circuits to which they may be applied most readily are indicated in Table 3-1.

Table 3-1: Recommended methods of finding Thévenin or Norton equivalents

Methods	Circuit contains		
			
R_{th} and v_{oc} or i_{sc}	✓	—	—
v_{oc} and i_{sc}	Possible	✓	—
$i = 1$ A or $v = 1$ V	—	—	✓

All possible methods do not appear in the table. We have used repeated source transformations on several networks when there were no dependent sources, and this is certainly an easy technique for networks that do not contain too many elements. Another method has a certain appeal because it can be used for any of the three types of networks tabulated in the foregoing. Simply replace the B network by a voltage source v_s, define the current leaving its positive terminal as i, then analyze the A network to obtain i, and put the equation in the form $v_s = ai + b$. Evidently, $a = R_{th}$ and $b = v_{oc}$. Of course, we could also apply a current source i_s, let its voltage be v, and then determine $v = ai_s + b$. This procedure is universally applicable, but some other method is usually easier and more rapid.

Although we are devoting our attention almost entirely to the analysis of *linear* circuits, its is enlightening to know that Thévenin's and Norton's theorems are both valid if network B is nonlinear; only network A must be linear.

Drill Problems

3-8. Find the Thévenin equivalent for the network of: (*a*) Fig. 3-30*a*; (*b*) Fig. 3-30*b*. *Ans:* 356 V, 40 Ω; $v_s/(1 - g_m R_1)$, $(R_1 + R_2)/(1 - g_m R_1)$

3-9. Find the Norton equivalent for the network of: (*a*) Fig. 3-30*c*; (*b*) Fig. 3-30*d*. *Ans:* 0 A, 14.6 Ω; 0.75 A, 26.7 Ω

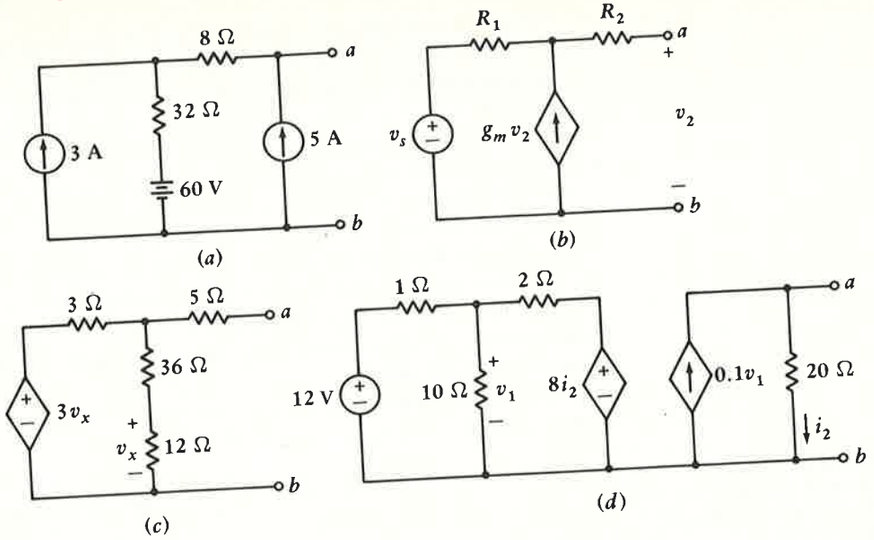


Fig. 3-30: See Drill Probs. 3-8 and 3-9.

3-7 Trees and general nodal analysis

In this section we shall generalize the method of nodal analysis that we have come to know and love. Since nodal analysis is applicable to any network, we cannot promise that we shall be able to solve a wider class of circuit problems. We can, however, look forward to being able to select a general nodal analysis method for any particular problem that may result in fewer equations and less work.

We must first extend our list of definitions relating to network topology. We begin by defining *topology* itself as a branch of geometry which is concerned with those properties of a geometrical figure which are unchanged when the figure is twisted, bent, folded, stretched, squeezed, or tied in knots, with the provision that no parts of the figure are to be cut apart or to be joined together. A sphere and a tetrahedron are topologically identical, as are a square and a circle. In terms of electric circuits, then, we are not now concerned with the particular types of elements appearing in the circuit, but only with the way in which branches and nodes are arranged. As a matter of fact, we usually suppress the nature of the elements and simplify the drawing of the circuit by showing the elements as lines. The resultant drawing is called a *linear graph*, or simply a *graph*. A circuit and its graph are shown in Fig. 3-31. Note that all nodes are identified by heavy dots in the graph.

Since the topological properties of the circuit or its graph are unchanged when it is distorted, the three graphs shown in Fig. 3-32 are all topologically identical with the circuit and graph of Fig. 3-31.

[7] This and the following section may be postponed if desired. They introduce analysis methods that are a little more general than those using node-to-reference voltages and mesh currents. Their use can lead to fewer equations or more useful current and voltage variables.

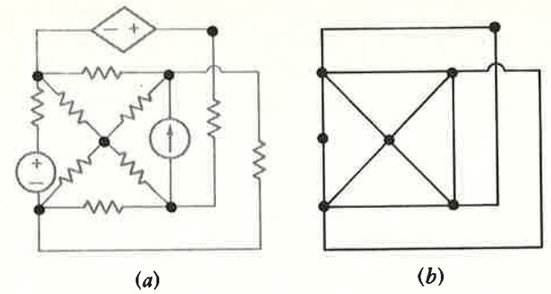


Fig. 3-31: (*a*) A given circuit. (*b*) The linear graph of this circuit.

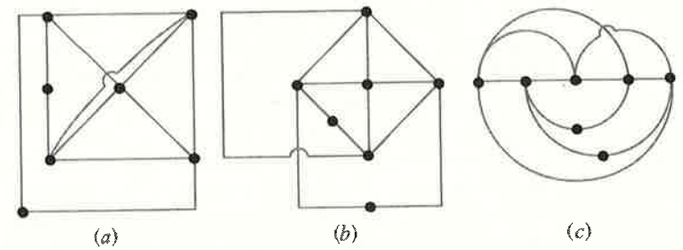


Fig. 3-32: The three graphs shown are topologically identical to each other and to the graph of Fig. 3-31*b*, and each is a graph of the circuit shown in Fig. 3-31a.

Topological terms which we already know and have been using correctly are:

node: a point at which two or more elements have a common connection.
path: a set of elements that may be traversed in order without passing through the same node twice.
branch: a single path, containing one simple element, which connects one node to any other node.
loop: a closed path.
mesh: a loop which does not contain any other loops within it.
planar circuit: a circuit which may be drawn on a plane surface in such a way that no branch passes over or under any other branch.
nonplanar circuit: any circuit which is not planar.

The graphs of Fig. 3-32 each contain 12 branches and 7 nodes.

Three new properties of a linear graph must now be defined, a tree, a cotree, and a link. We define a *tree* as any set of branches which does not contain any loops and yet connects every node to every other node, not necessarily directly. There are usually a number of different trees which may be drawn for a network, and the number increases rapidly as the complexity of the network increases. The simple graph shown in Fig. 3-33*a* has eight possible trees, four of which are shown by heavy lines in Figs. 3-33*b*, *c*, *d*, and *e*.

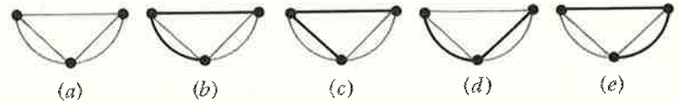


Fig. 3-33: (*a*) The linear graph of a three-node network. (*b*), (*c*), (*d*), and (*e*) Four of the eight different trees which may be drawn for this graph are shown by the heavy lines.

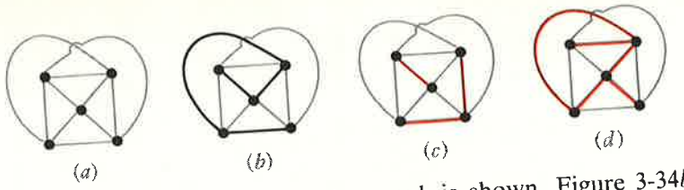


Fig. 3-34: (*a*) A linear graph. (*b*) A possible tree for this graph. (*c*) and (*d*) These sets of branches do not satisfy the definition of a tree.

In Fig. 3-34*a* a more complex graph is shown. Figure 3-34*b* shows one possible tree, and Figs. 3-34*c* and *d* show sets of branches which are *not* trees because neither set satisfies the definition above.

After a tree has been specified, those branches that are not part of the tree form the *cotree*, or complement of the tree. The lightly drawn branches in Figs. 3-33*b* to *e* show the cotrees that correspond to the heavier trees.

Once we understand the construction of a tree and its cotree, the concept of the link is very simple, for a *link* is any branch belonging to the cotree. It is evident that any particular branch may or may not be a link, depending on the particular tree which is selected.

The number of links in a graph may be related to the number of branches and nodes very simply. If the graph has N nodes, then exactly $(N - 1)$ branches are required to construct a tree because the first branch chosen connects two nodes and each additional branch includes one more node. Thus, given B branches, the number of links L must be

$$L = B - (N - 1) \tag{30}$$

or

$$L = B - N + 1$$

There are L branches in the cotree and $(N - 1)$ branches in the tree.

In any of the graphs shown in Fig. 3-33, we note that $3 = 5 - 3 + 1$, and in the graph of Fig. 3-34*b*, $6 = 10 - 5 + 1$. A network may be in several disconnected parts, and (30) may be made more general by replacing $+1$ with $+S$, where S is the number of separate parts. However, it is also possible to connect two separate parts by a *single* conductor, thus causing two nodes to form one node; no current can flow through this single conductor. This process may be used to join any number of separate parts, and thus we shall not suffer any loss of generality if we restrict our attention to circuits for which $S = 1$.

We are now ready to discuss a method by which we may write a set of nodal equations that are independent and sufficient. The method will enable us to obtain many different sets of equations for the same network, and all the sets will be valid. However, the method does not provide us with *every* possible set of equations. Let us first describe the procedure, illustrate it by three examples, and then point out the reason that the equations are independent and sufficient.

Given a network, we should:

1 Draw a graph and then identify a tree.
2 Place all voltage sources in the tree.
3 Place all current sources in the cotree.

4 Place all control-voltage branches for voltage-controlled dependent sources in the tree, if possible.
5 Place all control-current branches for current-controlled dependent sources in the cotree, if possible.

These last four steps effectively associate voltages with the tree and currents with the cotree.

We now assign a voltage variable (with its plus-minus pair) across each of the $(N - 1)$ branches in the tree. A branch containing a (dependent or independent) voltage source should be assigned that source voltage, and a branch containing a controlling voltage should be assigned that controlling voltage. The number of new variables that we have introduced is therefore equal to the number of branches in the tree $(N - 1)$, reduced by the number of voltage sources in the tree, and reduced also by the number of control voltages we were able to locate in the tree. In the third example below, we shall find that the number of new variables required may be zero.

Having a set of variables, we now need to write a set of equations that are sufficient to determine these variables. The equations are obtained through the application of KCL. Voltage sources are handled in the same way as in our earlier attack on nodal analysis; each voltage source and the two nodes at its terminals comprise a supernode or a part of a supernode. Kirchhoff's current law is then applied at all but one of the remaining nodes and supernodes. We set the sum of the currents leaving the node in all of the branches connected to it equal to zero. Each current is expressed in terms of the voltage variables we just assigned. One node may be ignored, just as was the case earlier for the reference node. Finally, in case there are current-controlled dependent sources, we must write an equation for each control current that relates it to the voltage variables; this also is no different from the procedure used before with nodal analysis.

Let us try out this process on the circuit shown in Fig. 3-35*a*. It contains four nodes and five branches, and its graph is shown in Fig. 3-35*b*. In accor-

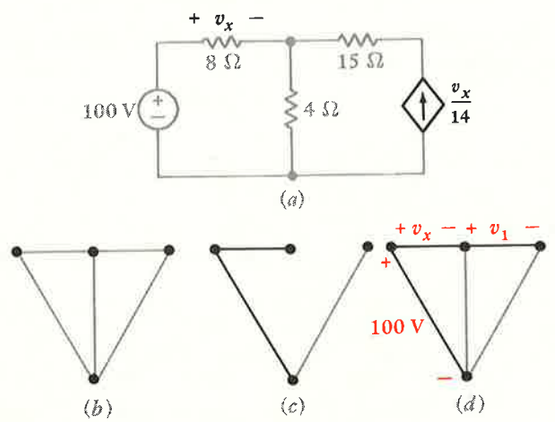


Fig. 3-35: (*a*) A circuit used as an example for general nodal analysis. (*b*) The graph of the given circuit. (*c*) The voltage source and the control voltage are placed in the tree, while the current source goes in the cotree. (*d*) The tree is completed and a voltage is assigned across each tree branch.

dance with steps 2 and 3 of the tree-drawing procedure, we place the voltage source in the tree and the current source in the cotree. Following step 4, we see that the v_x branch may also be placed in the tree since it does not form any loop which would violate the definition of a tree. We have now arrived at the two tree branches and the single link shown in Fig. 3-35*c*, and we see that we do not yet have a tree since the right node is not connected to the others by a path through tree branches. The only possible way to complete the tree is shown in Fig. 3-35*d*. The 100-V source voltage, the control voltage v_x, and a new voltage variable v_1 are next assigned to the three tree branches as shown.

We therefore have two unknowns, v_x and v_1, and it is obvious that we need to obtain two equations in terms of them. There are four nodes, but the presence of the voltage source causes two of them to form a single supernode. Kirchhoff's current law may be applied at any two of the three remaining nodes or supernodes. Let's attack the right node first. The current leaving to the left is $-v_1/15$, while that leaving downward is $-v_x/14$. Thus, our first equation is

$$-\frac{v_1}{15} - \frac{v_x}{14} = 0$$

The central node at the top looks easier than the supernode, so we set the sum of the current to the left, $-v_x/8$, the current to the right, $v_1/15$, and the downward current through the 4-Ω resistor equal to zero. This latter current is given by the voltage across the resistor divided by 4 Ω, but there is no voltage labeled on that link. However, when a tree is constructed according to the definition, there is a path through it from any node to any other node. Then, since every branch in the tree is assigned a voltage, we may express the voltage across any link in terms of the tree-branch voltages. This downward current is therefore $(-v_x + 100)/4$, and we have the second equation,

$$-\frac{v_x}{8} + \frac{v_1}{15} + \frac{-v_x + 100}{4} = 0$$

The simultaneous solution of these two nodal equations gives $v_1 = -60$ V, $v_x = 56$ V.

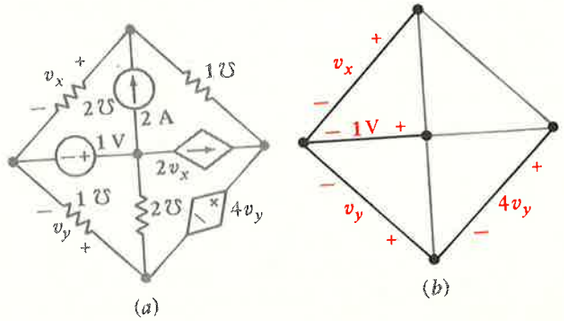


Fig. 3-36: (*a*) The circuit of Fig. 3-5 is repeated. (*b*) A tree is chosen such that both voltage sources and both control voltages are tree branches.

As a second example, let us reconsider a more complex circuit that we first analyzed by defining all node voltages with respect to a reference node. The circuit is that of Fig. 3-5, repeated as Fig. 3-36*a*. We draw a tree so that both voltage sources and both control voltages appear as tree-branch voltages and, hence, as assigned variables. As it happens, these four branches constitute a tree, Fig. 3-36*b*, and tree-branch voltages v_x, 1, v_y, and $4v_y$ are chosen, as shown.

Both voltage sources define supernodes and we apply KCL twice, once to the top node,

$$2v_x + 1(v_x - v_y - 4v_y) = 2$$

and once to the supernode consisting of the right node, the bottom node, and the dependent voltage source,

$$1v_y + 2(v_y - 1) + 1(4v_y + v_y - v_x) = 2v_x$$

Instead of the four equations we had previously, we have only two, and we find easily that $v_x = \frac{26}{9}$ V and $v_y = \frac{4}{3}$ V, both values agreeing with the earlier solution.

For a final example we consider the circuit of Fig. 3-37*a*. The two voltage sources and the control voltage establish the three-branch tree shown in Fig. 3-37*b*. Since the two upper and the lower right node all join to form one supernode, we need write only one KCL equation. Selecting the lower left node, we have

$$-1 - \frac{v_x}{4} + 3 + \frac{-v_x + 30 + 6v_x}{5} = 0$$

and it follows that $v_x = -\frac{32}{3}$ V. In spite of the apparent complexity of this circuit, the use of general nodal analysis has led to an easy solution. Employing mesh currents or node-to-reference voltages would require more equations and more effort.

We shall discuss the problem of finding the best analysis scheme in the following section.

If we should need to know some other voltage, current, or power in the previous example, one additional step would give the answer. For example, the power provided by the 3-A source is $3(-30 - \frac{32}{3}) = -122$ W.

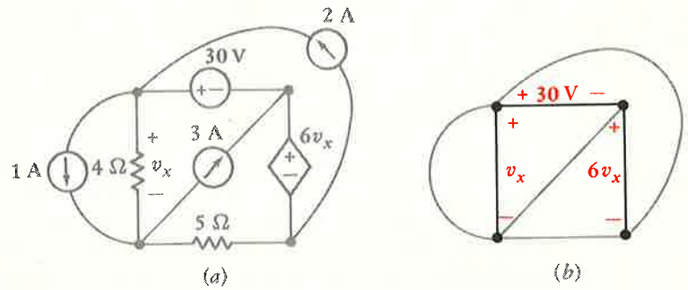


Fig. 3-37: (a) A circuit for which only one general nodal equation need be written. (*b*) The tree and the tree-branch voltages used.

Let us conclude by discussing the sufficiency of the assumed set of tree-branch voltages and the independence of the nodal equations. If these tree-branch voltages are *sufficient*, then the voltage of every branch in either the tree or the cotree must be obtainable from a knowledge of the values of all the tree-branch voltages. This is certainly true for those branches in the tree. For the links we know that each link extends between two nodes, and, by definition, the tree must also connect those two nodes. Hence, every link voltage may also be established in terms of the tree-branch voltages.

Once the voltage across every branch in the circuit is known, then all the currents may be found by using either the given value of the current if the branch consists of a current source, Ohm's law if it is a resistive branch, or by using KCL and these current values if the branch happens to be a voltage source. Thus, all the voltages and currents are determined and sufficiency is demonstrated.

To demonstrate independency, let us satisfy ourselves by assuming the situation where the only sources in the network are independent current sources. As we have noticed earlier, independent voltage sources in the circuit result in fewer equations, while dependent sources usually necessitate a greater number of equations. For independent current sources only, there will then be precisely $(N - 1)$ nodal equations written in terms of $(N - 1)$ tree-branch voltages. To show that these $(N - 1)$ equations are *independent*, visualize the application of KCL to the $(N - 1)$ different nodes. Each time we write the KCL equation, there is a new tree branch involved—the one which connects that node to the remainder of the tree. Since that circuit element has not appeared in any previous equation, we must obtain an independent equation. This is true for each of the $(N - 1)$ nodes in turn, and hence we have $(N - 1)$ independent equations.

Drill Problem

3-10. (*a*) How many trees may be constructed for the circuit of Fig. 3-38 that follow all five of the tree-drawing suggestions listed earlier? (*b*) Draw a suitable tree, write two equations in two unknowns, and find v_x. (*c*) What power is supplied by the dependent source? *Ans:* 1; 250 V; 20.5 kW

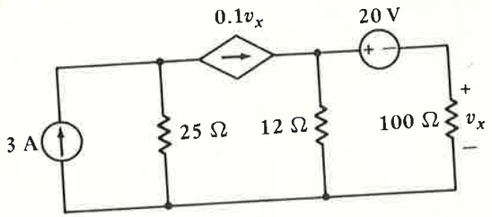


Fig. 3-38: See Drill Prob. 3-10.

3-8 Links and loop analysis

Now we shall consider the use of a tree to obtain a suitable set of loop equations. In some respects this is the dual of the method of writing nodal equations. Again it should be pointed out that, although we are able to guarantee that any set of equations we write will be both sufficient and independent, we should not expect that the method will lead directly to every possible set of equations.

We again begin by constructing a tree, and we use the same set of rules as we did for general nodal analysis. The objective either for nodal or loop analysis is to place voltages in the tree and currents in the cotree; this is a mandatory rule for sources and a desirable rule for controlling quantities.

Now, however, instead of assigning a voltage to each branch in the tree, we assign a current (including reference arrow, of course) to each element in the cotree or to each link. If there were ten links, we would assign exactly 10 link currents. Any link that contains a current source is assigned that source current as the link current. Note that each link current may also be thought of as a loop current, for the link must extend between two specific nodes, and there must also be a path between those same two nodes through the tree. Thus, with each link there is associated a single loop that includes that one link and a unique path through the tree. It is evident that the assigned current may be thought of either as a loop current or as a link current. The link connotation is most helpful at the time the currents are being defined, for one must be established for each link; the loop interpretation is more convenient at equation-writing time, because we shall apply KVL around each loop.

Let us try out this process of defining link currents by reconsidering an earlier example we worked using mesh currents. The circuit is shown in Fig. 3-12 and redrawn in Fig. 3-39*a*. The tree selected is one of several that might be constructed for which the voltage source is in a tree branch and the current source is in a link. Let us first consider the link containing the current source. The loop associated with this link is the left-hand mesh, so we show our link current flowing about the perimeter of this mesh, Fig. 3-39*b*. An obvious choice for the symbol for this link current is "7 A." Remember that no other current can flow through this particular link, and thus its value must be exactly the strength of the current source.

We next turn our attention to the 3-Ω resistor link. The loop associated with it is the upper right-hand mesh, and this loop (or mesh) current is defined as i_A and also shown in Fig. 3-39*b*. The last link is the lower 1-Ω resistor, and the only path between its terminals through the tree is around the perimeter of the circuit. That link current is called i_B, and the arrow indicating its path and reference direction appears in Fig. 3-39*b*. It is not a mesh current.

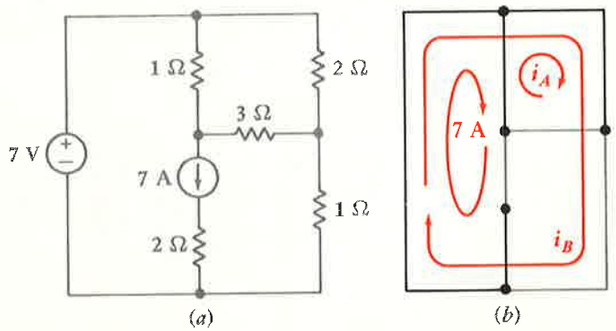


Fig. 3-39: (*a*) The circuit of Fig. 3-12 is shown again. (*b*) A tree is chosen such that the current source is in a link and the voltage source is in a tree branch.

Note that each link has only one current present in it, but a tree branch may have any number from one to the total number of link currents assigned. The use of long, almost closed, arrows to indicate the loops helps to indicate which loop currents flow through which tree branch and what their reference directions are.

A KVL equation must now be written around each of these loops. The variables used are the assigned link currents. Since the voltage across a current source cannot be expressed in terms of the source current, and since we have already used the value of the source current as the link current, we discard any loop containing a current source.

For the example of Fig. 3-39, we first traverse the i_A loop, proceeding clockwise from its lower left corner. The current going our way in the 1-Ω resistor is $(i_A - 7)$, in the 2-Ω element it is $(i_A + i_B)$, and in the link it is simply i_A. Thus

$$1(i_A - 7) + 2(i_A + i_B) + 3i_A = 0$$

For the i_B link, clockwise travel from the lower left corner leads to

$$-7 + 2(i_A + i_B) + 1i_B = 0$$

Traversal of the loop defined by the 7-A link is not required. Solving, we have $i_A = 0.5$ A, $i_B = 2$ A, once again. The solution has been achieved with one less equation than before.

An example containing a dependent source appears in Fig. 3-40*a*. This circuit contains six nodes, and its tree therefore must have five branches. Since there are eight elements in the network, there are three links in the

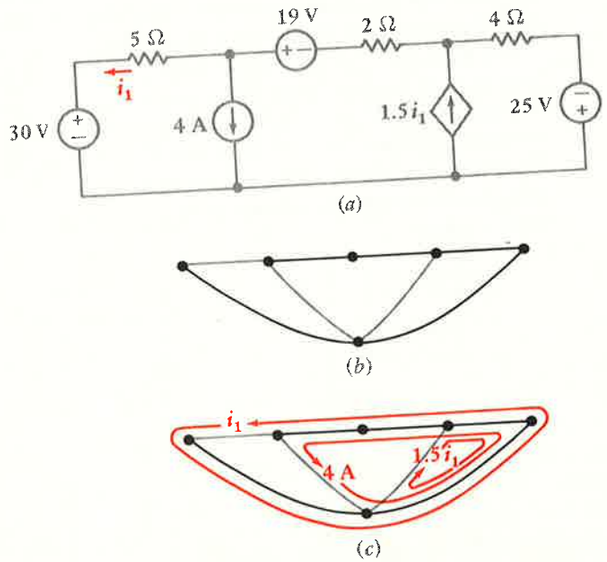


Fig. 3-40: (a) A circuit for which i_1 may be found with one equation using general loop analysis. (*b*) The only tree that satisfies the rules outlined in Sec. 3-7. (*c*) The three link currents are shown with their loops.

cotree. If we place the three voltage sources in the tree and the two current sources and the current control in the cotree, we are led to the tree shown in Fig. 3-40*b*. The source current of 4 A defines a loop as shown in Fig. 3-40*c*. The dependent source establishes the loop current $1.5i_1$ around the right mesh, and the control current i_1 gives us the remaining loop current about the perimeter of the circuit. Note that all three currents flow through the 4-Ω resistor.

We have only one unknown quantity, i_1, and, after discarding the loops defined by the two current sources, we apply KVL around the outside of the circuit:

$$-30 + 5(-i_1) + 19 + 2(-i_1 - 4) + 4(-i_1 - 4 + 1.5i_1) - 25 = 0$$

Besides the three voltage sources, there are three resistors in this loop. The 5-Ω resistor has one loop current in it since it is also a link, the 2-Ω resistor contains two loop currents, and the 4-Ω resistor has three. A carefully drawn set of loop currents is a necessity if errors in skipping currents, utilizing extra ones, or erring in the correct direction are to be avoided. The foregoing equation is guaranteed, however, and it leads to $i_1 = -12$ A.

How may we demonstrate sufficiency? Let us visualize a tree. It contains no loops and therefore contains at least two nodes to each of which only one tree branch is connected. The current in each of these two branches is easily found from the known link currents by applying KCL. If there are other nodes at which only one tree branch is connected, these tree-branch currents may also be immediately obtained. In the tree shown in Fig. 3-41, we thus have found the currents in branches *a*, *b*, *c*, and *d*. Now we move along the branches of the tree, finding the currents in the tree branches *e* and *f*; the process may be continued until all the branch currents are determined. The link currents are therefore sufficient to determine all branch currents. It is helpful to look at the situation where an incorrect "tree" has been drawn which contains a loop. Even if all the link currents were zero, a current might still circulate about this "tree loop." Hence, the link currents could not determine this current, and they would not represent a sufficient set. Such a "tree" is by definition impossible.

To demonstrate independence, let us satisfy ourselves by assuming the situation where the only sources in the network are independent voltage sources. As we have noticed earlier, independent current sources in the circuit result in fewer equations, while dependent sources usually necessi-

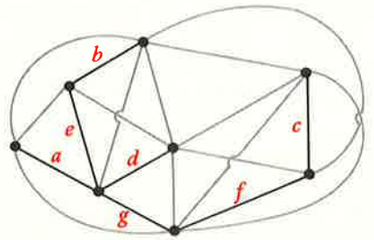


Fig. 3-41: A tree which is used as an example to illustrate the sufficiency of the link currents.

tate a greater number of equations. For independent voltage sources only, there will then be precisely $(B - N + 1)$ loop equations written in terms of the $(B - N + 1)$ link currents. To show that these $(B - N + 1)$ loop equations are independent, it is only necessary to point out that each represents the application of KVL around a loop which contains one link not appearing in any other equation. We might visualize a different resistance $R_1, R_2, \ldots, R_{B-N+1}$ in each of these links, and it is then apparent that one equation can never be obtained from the others since it contains one coefficient not appearing in any other equation.

Hence, the link currents are sufficient to enable a complete solution to be obtained, and the set of loop equations which we use to find the link currents is a set of independent equations.

Having looked at both general nodal analysis and loop analysis, we should now consider the advantages and disadvantages of each method so that an intelligent choice of a plan of attack can be made.

The nodal method in general requires $(N - 1)$ equations, but this number is reduced by one for each independent or dependent voltage source in a tree branch, and increased by one for each dependent source that is voltage controlled by a link voltage or current controlled.

The loop method basically involves $(B - N + 1)$ equations. However, each independent or dependent current source in a link reduces this number by one, while each dependent source that is current controlled by a tree-branch current or is voltage controlled increases the number by one.

As a grand finale for this discussion, let us inspect the T-equivalent-circuit model for a transistor, shown in Fig. 3-42, to which are connected a sinusoidal source, 4 sin 1000t mV, and a 10-kΩ load. We select typical values for the emitter resistance, $r_e = 50\ \Omega$; for the base resistance, $r_b = 500\ \Omega$; for the collector resistance, $r_c = 20$ kΩ; and for the common-base forward-current-transfer ratio, $\alpha = 0.98$. Suppose that we wish to find the input (emitter) current i_e and the load voltage v_L.

Although the details are requested in Drill Probs. 3-12 and 3-13 below, we should see readily that the analysis of this circuit might be accomplished by drawing trees requiring three general nodal equations $(N - 1 - 1 + 1)$ or two loop equations $(B - N + 1 - 1)$. We might also note that three equations are required in terms of node-to-reference voltages, as are three mesh equations.

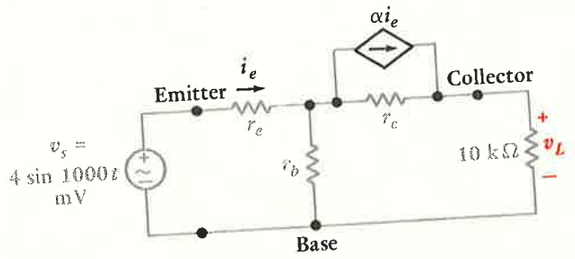


Fig. 3-42: A sinusoidal voltage source and a 10-kΩ load are connected to the T-equivalent circuit of a transistor. The common connection between the input and output is at the base terminal of the transistor and the arrangement is called the common-base configuration.

No matter which method we choose, these results are obtained for this specific circuit:

$$i_e = 18.14 \sin 1000t \quad \mu\text{A}$$

$$v_L = 119.6 \sin 1000t \quad \text{mV}$$

and we therefore find that this transistor circuit provides a voltage gain (v_L/v_s) of 29.9, a current gain ($v_L/10\,000 i_e$) of 0.659, and a power gain equal to the product, 29.9 (0.659) = 19.70. Higher gains could be secured by operating this transistor in a common-emitter configuration, as illustrated by the equivalent circuit of Prob. 42.

Drill Problems

3-11. Draw a suitable tree and use general loop analysis to find i_A in the circuit of: (*a*) Fig. 3-43*a* by writing just one equation with i_A as the variable; (*b*) Fig. 3-43*b* by writing just two equations with i_A and i_B as the variables.

Ans: 1.6; 9.39 A

3-12. For the transistor amplifier equivalent circuit shown in Fig. 3-42, let $r_e = 50\ \Omega$, $r_b = 500\ \Omega$, $r_c = 20$ kΩ, $\alpha = 0.98$, and find both i_e and v_L by drawing a suitable tree and using: (*a*) two loop equations; (*b*) three nodal equations with a common reference node for the voltages; (*c*) three nodal equations without a common reference node.

Ans: 18.14 sin 1000t mA; 119.6 sin 1000t mV

3-13. Determine the Thévenin and Norton equivalent circuits presented to the 10-kΩ load in Fig. 3-42 by finding: (*a*) the open-circuit value of v_L; (*b*) the (downward) short-circuit current; (*c*) the Thévenin equivalent resistance. All circuit values are given in Drill Prob. 3-12.

Ans: 146.2 sin 1000t mV; 65.6 sin 1000t μA; 2.23 kΩ

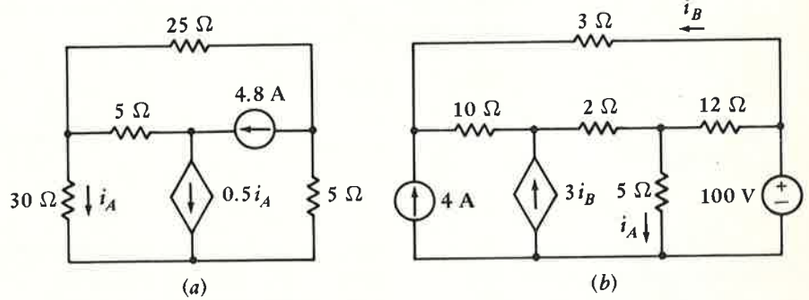


Fig. 3-43: See Drill Prob. 3-11.

Problems

1 (*a*) Find v_2 if $v_1 + 2v_2 + 3v_3 = 20$, $v_1 - 7v_2 - 5v_3 = -5$, and $v_3 + 3v_2 + 4v_1 - 10 = 0$. (*b*) Evaluate the determinant:

$$\begin{vmatrix} 1 & 2 & 3 & 4 \\ 2 & 3 & 4 & 1 \\ 3 & 4 & 1 & -2 \\ 4 & -1 & 2 & 3 \end{vmatrix}$$

2 Use nodal analysis to find v_P in the circuit shown in Fig. 3-44.

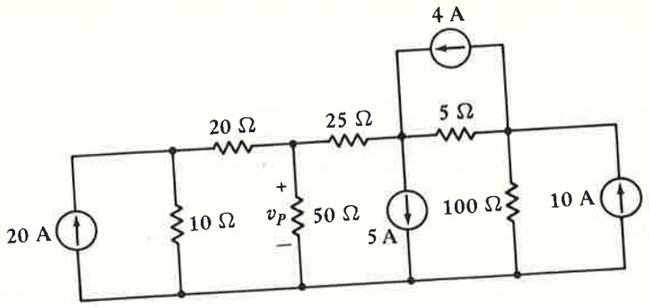


Fig. 3-44: See Prob. 2.

3 Use nodal analysis on the circuit given in Fig. 3-45 to find: (*a*) v_3; (*b*) the power being supplied by the 5-A source.

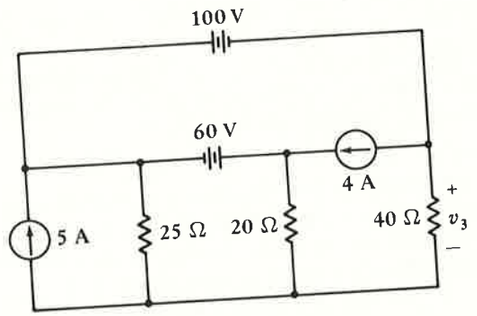


Fig. 3-45: See Prob. 3.

4 Make use of nodal analysis to find v_x and the power delivered to the 50-Ω resistor in the circuit of Fig. 3-46.

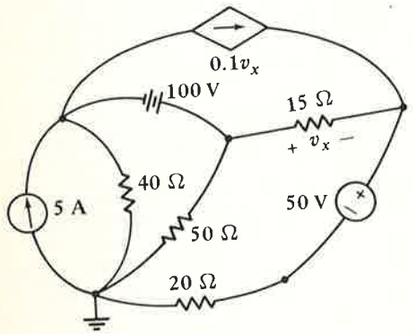


Fig. 3-46: See Prob. 4.

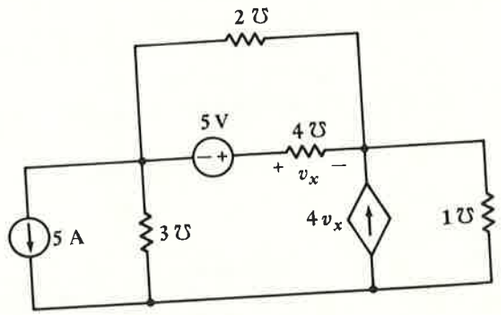


Fig. 3-47: See Prob. 5.

5 Set up nodal equations for the circuit illustrated in Fig. 3-47, and then find the power supplied by the 5-V source.

6 Use nodal analysis to find v_x in the circuit of Fig. 3-48.

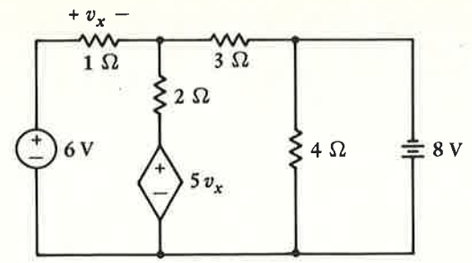


Fig. 3-48: See Probs. 6, 12, and 28.

7 Analyze the circuit of Fig. 3-49 using node voltages and find the power being supplied by the 6-A source.

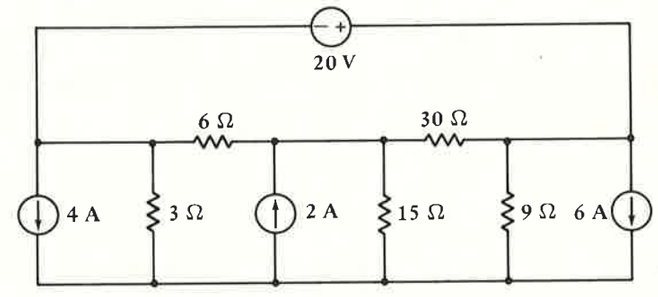


Fig. 3-49: See Prob. 7.

8 In Fig. 3-50, find v_2 through the use of nodal analysis.

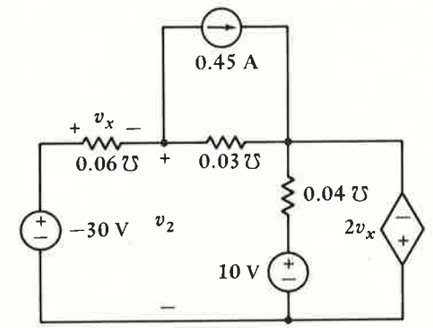


Fig. 3-50: See Prob. 8.

9 In the circuit of Fig. 3-51, use mesh analysis to: (*a*) find the power delivered to the 4-Ω resistor. (*b*) To what voltage should the 100-V battery be changed so that no power is delivered to the 4-Ω resistor?

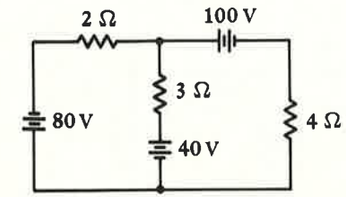


Fig. 3-51: See Prob. 9.

10 Use mesh analysis on the circuit shown in Fig. 3-52 to find the power supplied by the 4-V battery.

11 In Fig. 3-53, every resistance is 6 Ω and every battery voltage is 12 V. Find i_A.

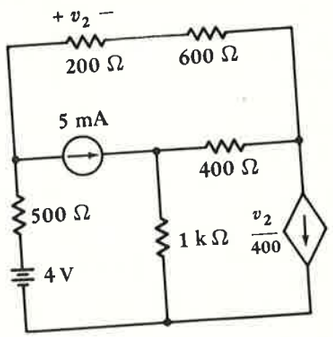


Fig. 3-52: See Prob. 10.

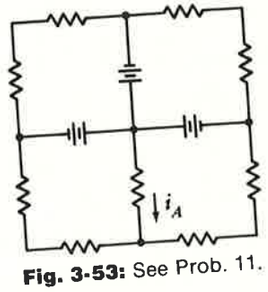


Fig. 3-53: See Prob. 11.

12 In the circuit of Fig. 3-48, change the right-hand element to an 8-A independent current source, arrow directed upward, and use mesh analysis to find the power absorbed by the 3-Ω resistor.

13 Use mesh analysis on the circuit of Fig. 3-54 to find the values of all the mesh currents.

14 In the circuit of Fig. 3-4*b*, use mesh analysis to find i_o, the current flowing downward in R_L if $v_2 = 1.234\ 321$ V.

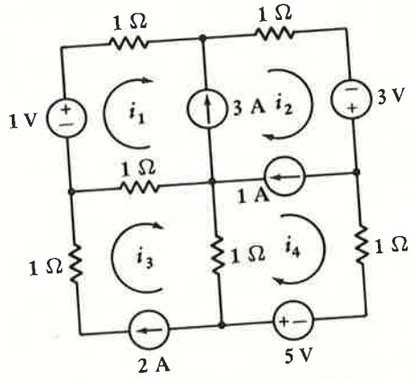


Fig. 3-54: See Prob. 13.

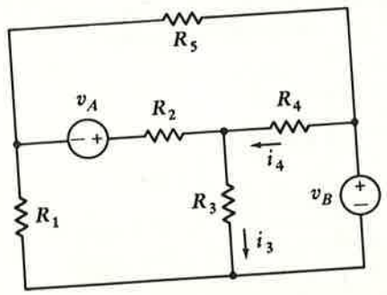


Fig. 3-55: See Prob. 15.

15 In the circuit shown in Fig. 3-55: (*a*) if $v_A = 20$ V and $v_B = 0$, $i_3 = 1.5$ A; find i_3 if $v_A = 50$ V and $v_B = 0$; (*b*) if $v_A = 20$ V and $v_B = 50$ V, $i_4 = 2$ A, while $i_4 = -1$ A if $v_A = 50$ V and $v_B = 20$ V; find i_4 if $v_A = 30$ V and $v_B = 100$ V.

16 Use superposition with the circuit of Fig. 3-56 to find i_x.

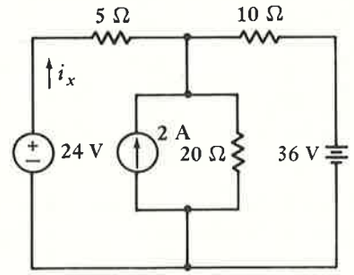


Fig. 3-56: See Prob. 16.

17 With reference to the circuit outlined in Fig. 3-57, when $v_s = 120$ V, it is found that $i_1 = 3$ A, $v_2 = 50$ V, and the power delivered to R_3 is 60 W. If Con Ed reduces v_s to 105 V, find new values for i_1, v_2, and the power delivered to R_3.

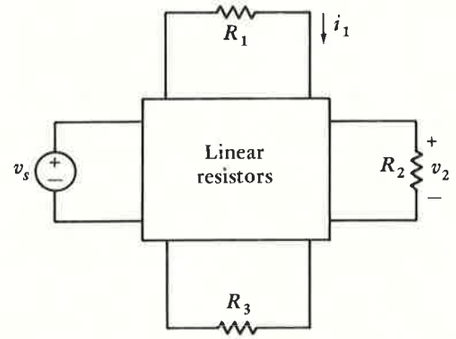


Fig. 3-57: See Prob. 17.

18 Use the superposition theorem on the circuit shown in Fig. 3-58 to find i.

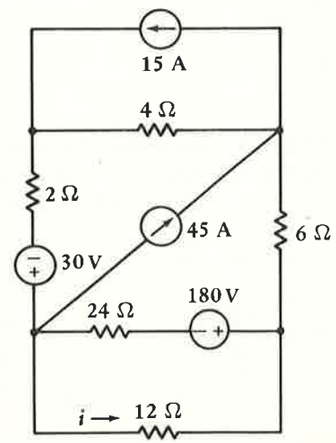


Fig. 3-58: See Prob. 18.

19 The circuit illustrated in Fig. 3-59 contains a dependent source. Use the superposition theorem to find the current I.

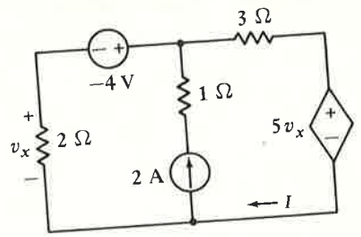


Fig. 3-59: See Probs. 19 and 29.

20 In the circuit of Fig. 3-60, use superposition to help find the power absorbed by the: (*a*) 6-V source; (*b*) 3-A source; (*c*) 12-V source; (*d*) 2-A source.

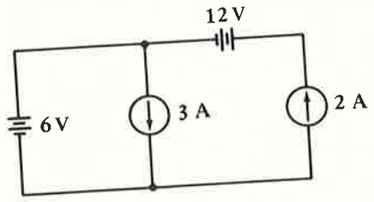


Fig. 3-60: See Prob. 20.

21 A Radio Shack type 222 flashlight bulb is intended for use with two 1.55-V penlight (AA) batteries in series. The bulb, however, is marked "2.25 V, 0.25 A." Assuming all markings are correct, what practical voltage source might be used to model one of the batteries?

22 By making repeated source transformations and resistance combinations for each network in Fig. 3-61, replace the network to the left of terminals *a-b* with the series combination of a single independent voltage source and a single resistor.

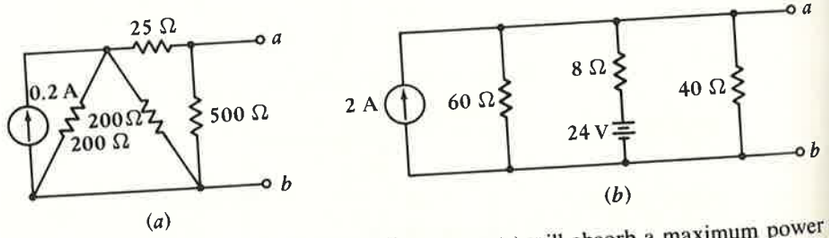


Fig. 3-61: See Prob. 22.

23 In the circuit of Fig. 3-62, what value of R_L: (*a*) will absorb a maximum power from this network and what is $p_{L,\max}$? (*b*) will have the maximum voltage across it and what is $v_{L,\max}$? (*c*) will have a maximum current through it and what is $i_{L,\max}$?

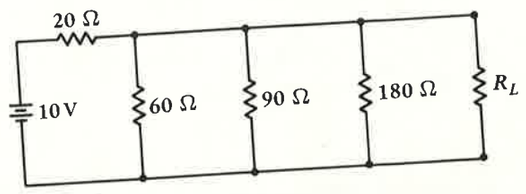


Fig. 3-62: See Prob. 23.

24 Consider the practical voltage source to the left of terminals *a-b* in Fig. 3-63. (*a*) What must be the value of R_L to cause the maximum possible power to be drawn from the *practical source?* (*b*) What is the value of this maximum power?

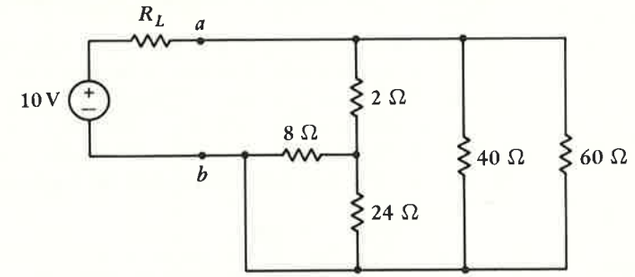


Fig. 3-63: See Prob. 24.

25 (*a*) Use three separate analyses to find v_{oc}, i_{sc}, and R_{th} with respect to terminals *a-b* for the circuit shown in Fig. 3-64. (*b*) Draw the Thévenin and Norton equivalents as seen at *a-b*.

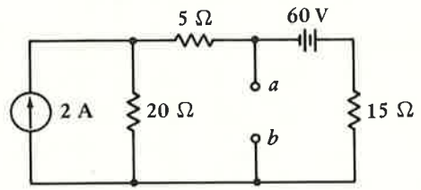


Fig. 3-64: See Prob. 25.

26 Find the Thévenin equivalent circuit with respect to terminals *a-b* for the circuit shown in Fig. 3-65.

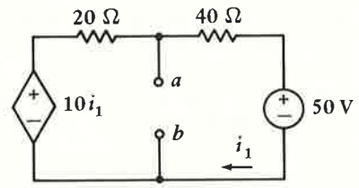


Fig. 3-65: See Probs. 26 and 30.

27 (*a*) Determine the Thévenin and Norton equivalent circuits as seen at terminals *a-b* for the network of Fig. 3-66. (*b*) Replace the 5-A source with a dependent voltage source labeled $5i_x$ (+ reference at the right) and again find the Thévenin and Norton equivalents.

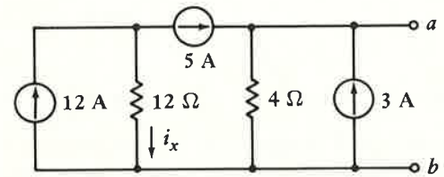


Fig. 3-66: See Prob. 27.

28 In the circuit of Fig. 3-48, find the Thévenin equivalent of the network: (*a*) to the left of the 8-V source; (*b*) to the right of the 6-V source.

29 (*a*) Refer to the circuit shown in Fig. 3-59 and find the Thévenin equivalent circuit faced by the 3-Ω resistor. (*b*) Find I. (*c*) Change the 3-Ω resistor to 13 Ω and again find I.

30 If the voltage v_L across or the current $i_L = v_L/R_L$ through a general load resistance R_L is known, then the Thévenin or Norton equivalent may be determined easily since $v_{oc} = \lim_{R_L \to \infty} v_L$ and $i_{sc} = \lim_{R_L \to 0} i_L$. (*a*) Find v_L (+ sign at terminal "*a*") for the circuit of Fig. 3-65 if a resistance R_L is connected between a and b. (*b*) Use The expressions above to determine v_{oc} and i_{sc}.

31 Find the Thévenin equivalent circuit for the network shown in Fig. 3.67.

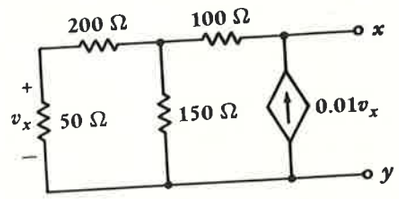


Fig. 3-67: See Prob. 31.

32 Determine the Thévenin equivalent circuit of the network shown in Fig. 3-68.

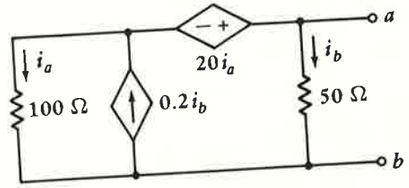


Fig. 3-68: See Prob. 32.

33 The voltage follower shown in Fig. 3-28 is modified by inserting a finite R_i = 10 kΩ between the terminals across which v_i is defined. Find the new Thévenin equivalent.

34 (*a*) Construct all possible trees for the linear graph shown in Fig. 3-69. (*b*) If the top two branches are voltage sources and the left branch is a current source, show all possible trees.

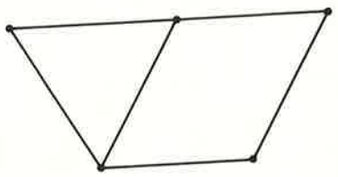


Fig. 3-69: See Prob. 34.

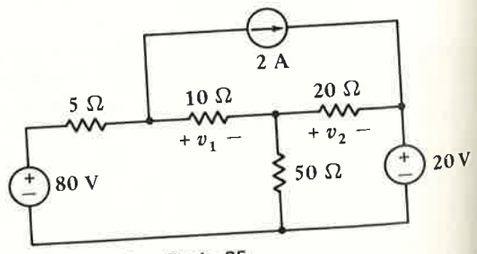


Fig. 3-70: See Prob. 35.

35 For the circuit shown in Fig. 3-70, construct a tree in which v_1 and v_2 are tree-branch voltages, write nodal equations, and solve for v_1.

36 Construct a suitable tree for the circuit of Fig. 3-71, assign tree-branch voltages, write KCL and control equations, and find i_2.

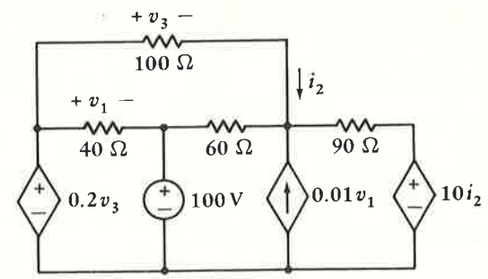


Fig. 3-71: See Prob. 36.

37 Use nodal analysis with tree-branch voltages on the circuit of Fig. 3-72 to determine what value of V_2 will cause $v_z = 0$.

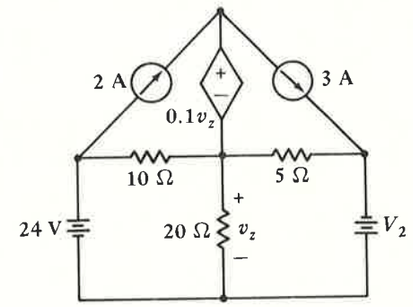


Fig. 3-72: See Prob. 37.

38 For the circuit shown in Fig. 3-73, construct a tree in which i_1 and i_2 are link currents, write loop equations, and evaluate i_1 and i_2.

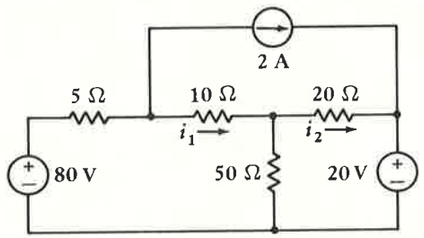


Fig. 3-73: See Prob. 38.

39 (*a*) Construct a suitable tree for the circuit of Fig. 3-74 and write the single equation necessary to find i_1. (*b*) Find i_1.

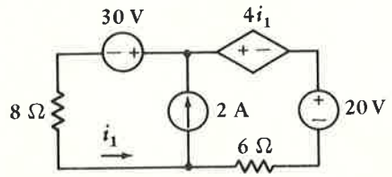


Fig. 3-74: See Prob. 39.

40 Devise a tree for the circuit shown in Fig. 3-75 for which all loop currents flow through the 1-Ω resistor. Find i.

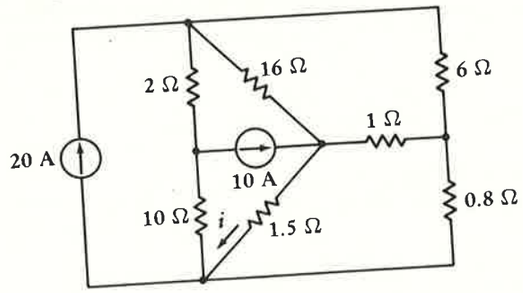


Fig. 3-75: See Prob. 40.

41 Use general loop analysis on the nonplanar circuit of Fig. 3-76 to find i_x.

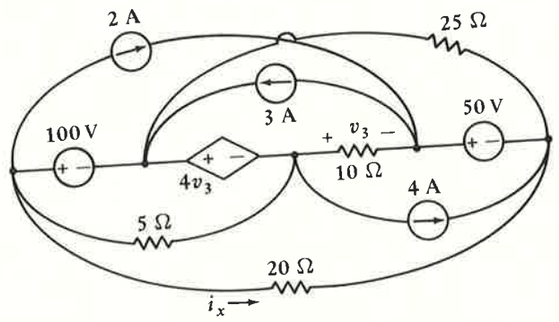


Fig. 3-76: See Prob. 41.

42 Figure 3-77 shows one form of the equivalent circuit for a transistor amplifier. Determine the open-circuit value of v_2 and the output resistance (R_{th}) of the amplifier.

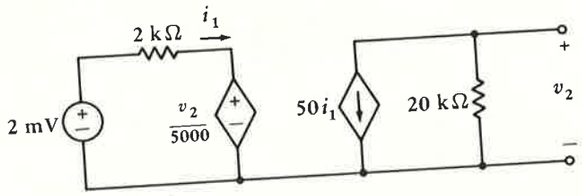


Fig. 3-77: See Prob. 42.

PART TWO
THE TRANSIENT CIRCUIT