6.200 Circuits and Electronics

Week 7 Recitation:
Operational Amplifiers

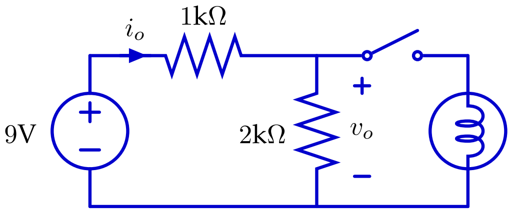
Grab participation sheet by the door.

Midterm: next Tuesday (review materials on web).

No p-set this week.

Loading

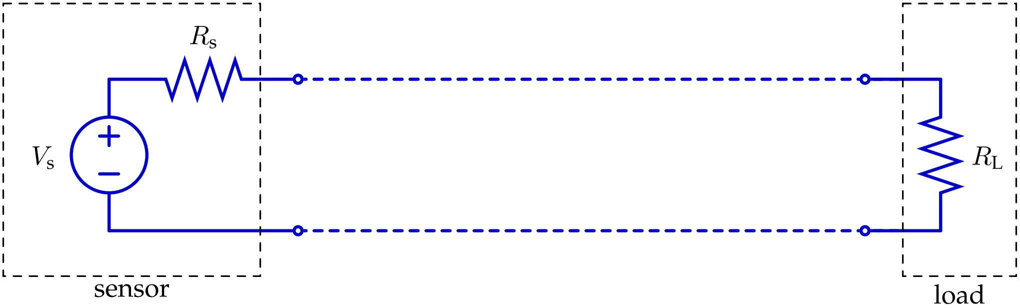
Circuit design is complicated by interactions among the elements. Adding an element changes voltages and current *throughout* the circuit. For example, what happens when the switch is closed in the following circuit (effectively adding the light bulb as a new component)?



0. v_o and i_o stay the same
1. v_o decreases, i_o decreases
2. v_o decreases, i_o increases
3. v_o increases, i_o decreases
4. v_o increases, i_o increases
5. depends on the bulb's resistance

Memories...

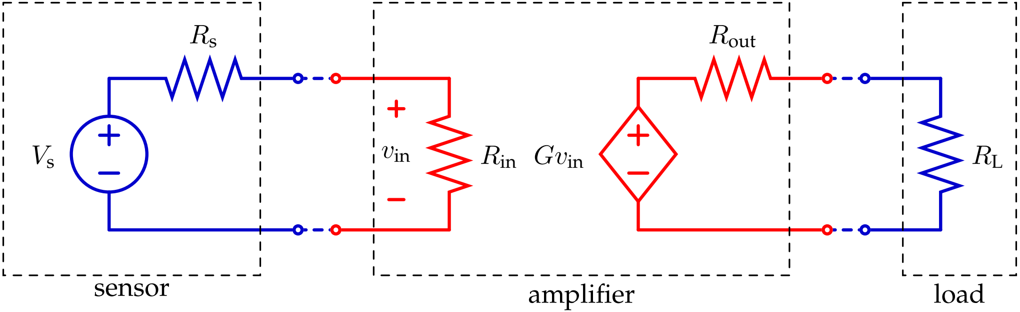
Consider an arbitrary sensor with a small output voltage, driving a load of some kind:



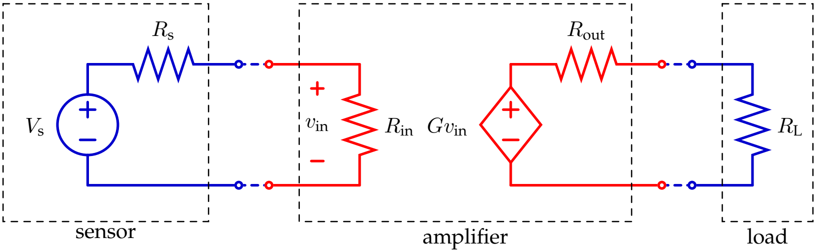
What is the problem here?

Amplifiers

We could resolve this issue by building a circuit that behaves like the following, to isolate the sensor and the load (and also scale up the sensor's voltage):



Check Yourself

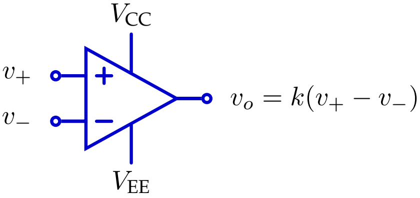


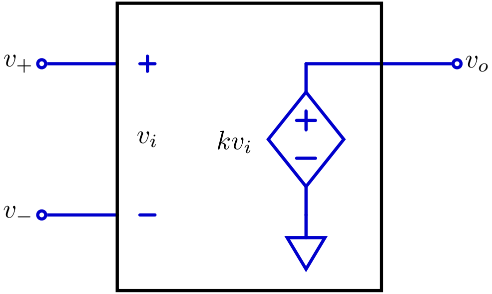
For this amplifier to work as well as possible, what should R_{in} and R_{out} be?

1. R_{in} small, R_{out} small
2. R_{in} small, R_{out} big
3. R_{in} big, R_{out} small
4. R_{in} big, R_{out} big

Operational Amplifiers

An operational amplifier (“op-amp”) can be modeled* as a voltage-controlled voltage source, where k is intentionally large (typically $\sim 10^5 - 10^7$):

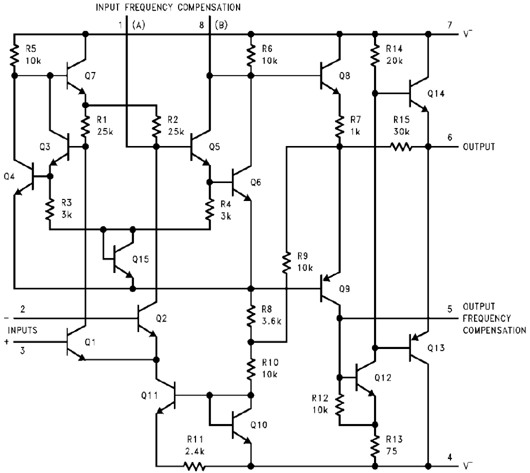




* sometimes

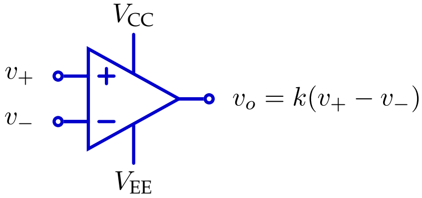
Operational Amplifiers

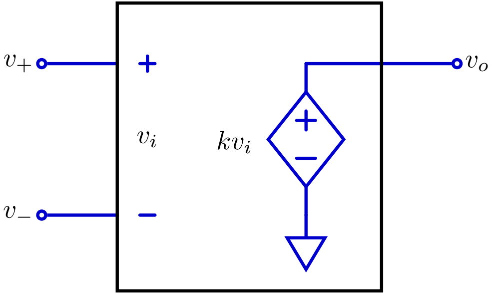
What's *actually* in an op-amp? Here is a more accurate circuit model of a μA709 op-amp:



But that's a pain...

Characterizing an Op-amp (VCVS Model)



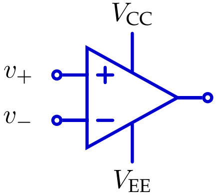


Sketch a graph of v_o versus $(v_+ - v_-)$

Supply Rails

Op-amps derive power from connections to a power supply, and the output voltage is typically constrained by that power supply:

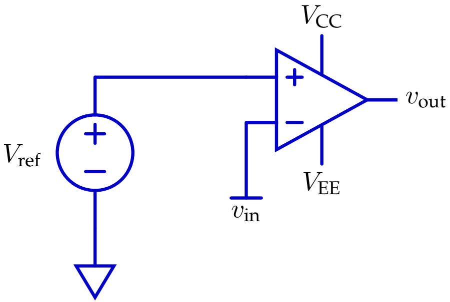
$$V_{\text{EE}} < v_o < V_{\text{CC}}$$



$$v_o = \begin{cases} V_{\text{CC}} & \text{if } k(v_+ - v_-) > V_{\text{CC}} \quad \text{(positive saturation region)} \\ V_{\text{EE}} & \text{if } k(v_+ - v_-) < V_{\text{EE}} \quad \text{(negative saturation region)} \\ k(v_+ - v_-) & \text{otherwise} \quad \text{(linear region)} \end{cases}$$

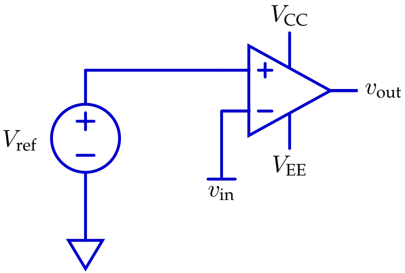
Op-Amps as Comparators

Other than the (tiny) range of $v_+ - v_-$ values where we're operating in the linear region, the op-amp's output voltage will be forced to one or the other of the supply rails, so the op-amp naturally behaves as a comparator:



Under what conditions is the output equal to V_{CC}?
Under what conditions is the output equal to V_{EE}?

Check Yourself



Consider this circuit again, where:

- $V_{CC} = 5\text{V}$
- $V_{EE} = -5\text{V}$
- $V_{ref} = 0\text{V}$
- $v_{in}(t) = \sin(t)$

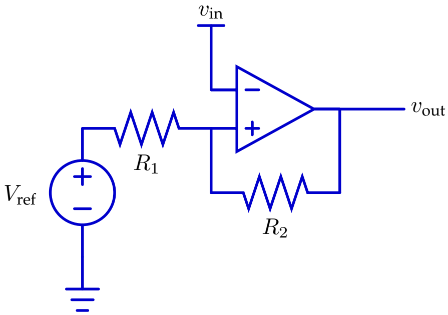
Sketch the input $v_{in}(t)$ and the output $v_{out}(t)$ on the same axes.

Comparator in Practice

See `rec07.py`.

Dealing with Noise

We can deal with the effect of this noise by adding some *hysteresis* into our system. Practically, we will be changing V_{ref} based on the current value of the output using the following topology:



Notice that the value of v_+ changes as v_{out} changes.

What is v_+ when $v_{\text{out}} = V_{\text{CC}}$?
What is v_+ when $v_{\text{out}} = V_{\text{EE}}$?
How would this change affect your graph from the previous slide?